N-Channel Enhancement Mode MOSFET

Features

For a single mosfet

$V_{DS(V)}$= 60V，I_D= 0.5A

$R_{DS(ON)}$ <2Ω，@V_{GS} = 10V, I_D=0.5A

$R_{DS(ON)}$ <4Ω，@V_{GS} = 4.5V, I_D=0.2A

Very low level gate drive requirements allowing direct

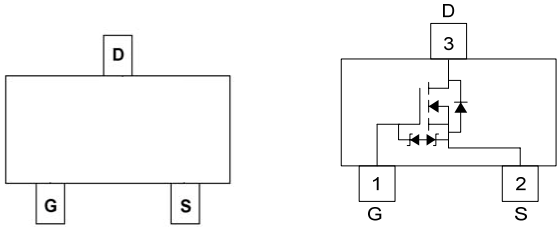
Gate-Source Zener for ESD ruggedness，>2kV Human Body Model

General Description

These N-Channel logic level enhancement mode field effect transistors are produced using Fairchild 's proprietary high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance.

This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, these N-Channel FET's can replace several digital transistors, with a variety of bias resistors.

Pin Configuration



SOT23

Absolute Maximum Ratings @ T_A = 25°C unless otherwise specified

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous @ T_J = 25 °C	—Continuous	I_D	0.5	A
	—Pulsed[b]	I_{DM}	1.5	A
Drain-Source Diode Forward Current[a]		I_S	0.55	A
Maximum Power Dissipation[a]		P_D	0.9	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)		ESD	2.0	KV

Notes：

a. Mounted on a 1in2 FR-4board with 2oz, Copper in a still air environment at 25°C,the current rating is based on the DC(<10s) test conditions, for each single die.

b. Pulse test: Pulse Width<300us,Duty Cycle<2%.

- **Electrical Characteristics** @ T_A = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	60		--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	--		1	uA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	--		±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250uA	1.0		2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 0.5A			2	Ω
		V_{GS} = 4.5V, I_D = 0.2A			4	
Forward Transconductance	G_{FS}	V_{DS} = 10V, I_D = 0.2A		0.2		S
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V F = 1.0MHz	--	9.5	--	pF
Output Capacitance	C_{OSS}		--	6		
Reverse Transfer Capacitance	C_{RSS}			1.5		
Total Gate Charge	Q_G	V_{DS} = 25V, I_D = 0.2A, V_{GS} = 10V		0.5	0.7	nC
Gate-Source Charge	Q_{GS}			0.22		
Gate-Drain	Q_{GD}			0.07		
Turn-On Delay Time	$T_{D(ON)}$	V_{DD} =30V, I_D = 0.5A, V_{GS} = 10V, R_{GEN} = 10Ω	--	5	10	nS
Turn-Off Delay Time	$T_{D(OFF)}$			4	8	
Turn-On Rise Time	T_r			4.5	10	
Turn-Off Fall Time	T_f			3.2	7	

- **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

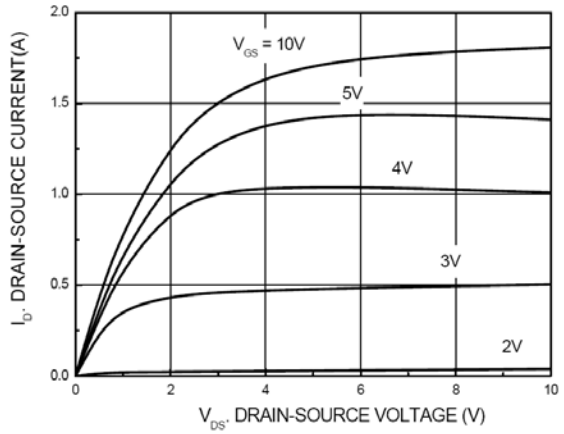


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

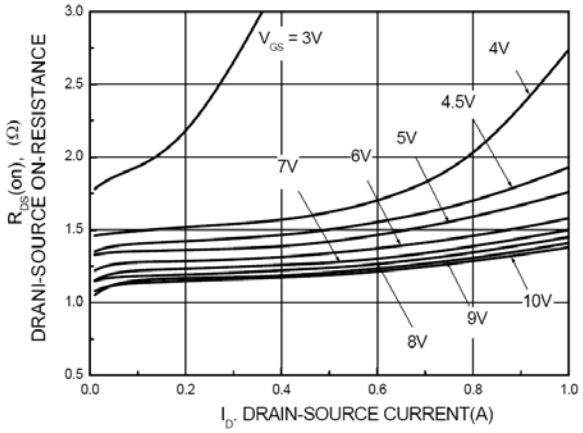


Figure 3. On-Resistance Variation with Temperature

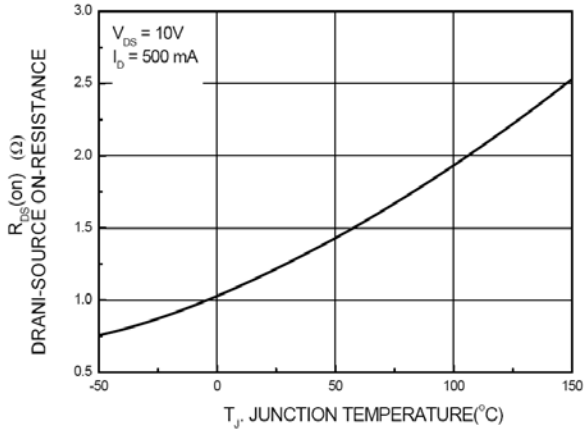


Figure 4. On-Resistance Variation with Gate-Source Voltage

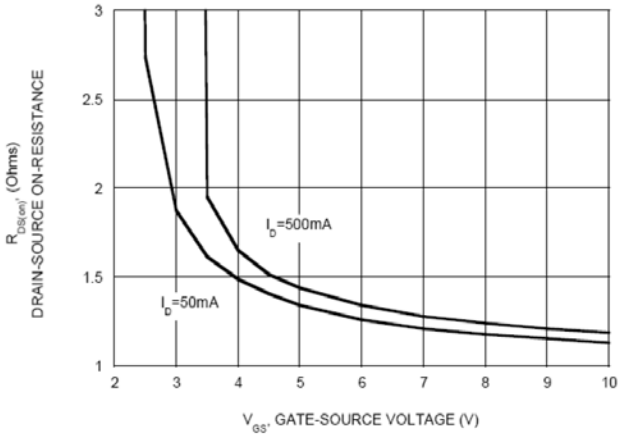


Figure 5. Transfer Characteristics

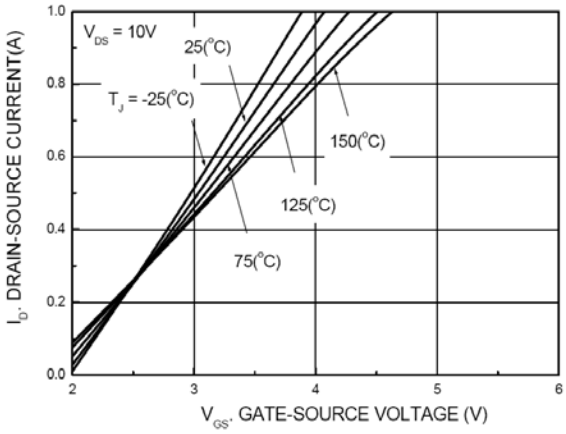
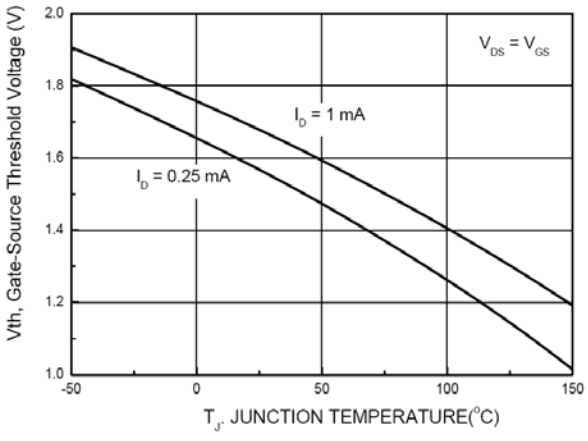
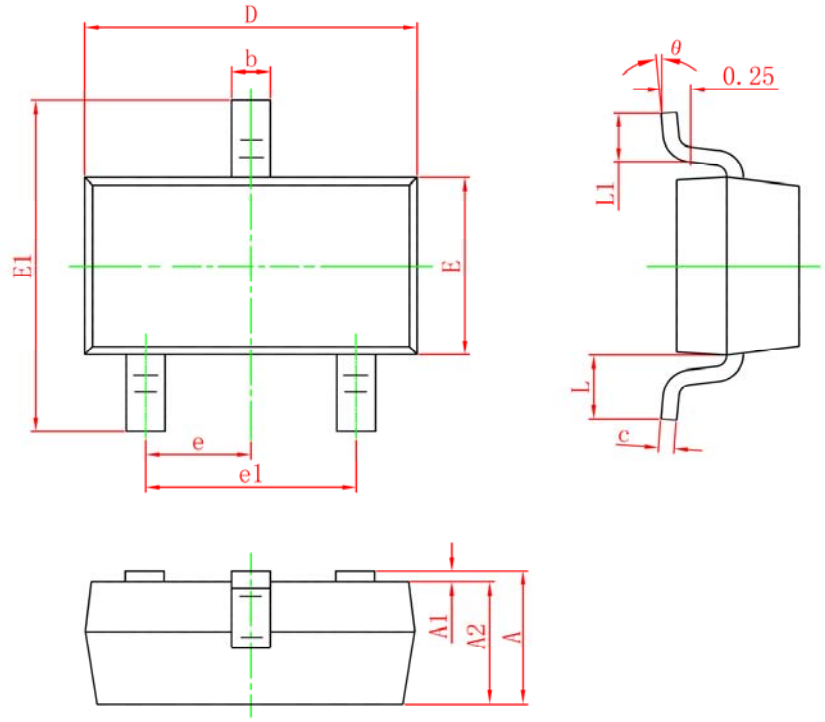


Figure 6. Gate Threshold Variation with Temperature



- **Package Information**

SOT-23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°
UNIT:mm				