P-Channel 30V (D-S) MOSFET

Features

-30V/-4.5A,$R_{DS(ON)}$=60mΩ@V_{GS}=-10V
-30V/-3.7A,$R_{DS(ON)}$=90mΩ@V_{GS}=-4.5V
Super high density cell design for
extremely low $R_{DS(ON)}$
Exceptional on-resistance and maximum DC current capability

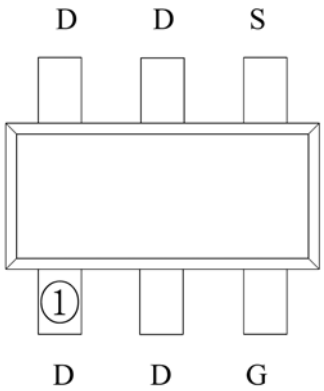
General Description

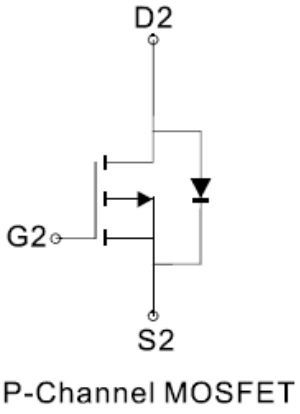
The FS5905 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Applications

Power Management in Note book
Portable Equipment
Battery Powered System
DC/DC Converter
Load Switch
DSC
LCD Display inverter

Pin Configurations





P-Channel MOSFET

- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

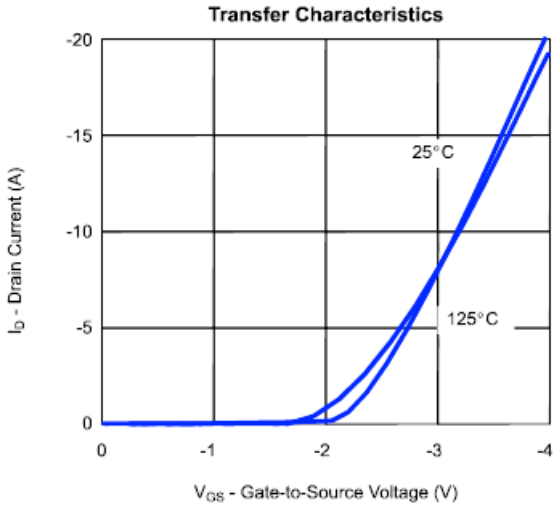
Parameter		Symbol	Limits	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (t_j=150)	T_a=25	I_D	-4.5	A
	T_a=70		-3.6	
Pulsed Drain Current[1)]		I_{DM}	-30	A
Continuous Drain Current (Diode Conduction)		I_s	-1.7	A
Maximum Power Dissipation	T_A=25	P_D	1.25	W
	T_A=70		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Storage Temperature Range		T_{stg}	-55 to 150	
Thermal Resistance- Junction-to-Ambient *		R_{JA}	42	W
			Steady State 55	
Thermal Resistance- Junction-to-Case		R_{Jc}	35	

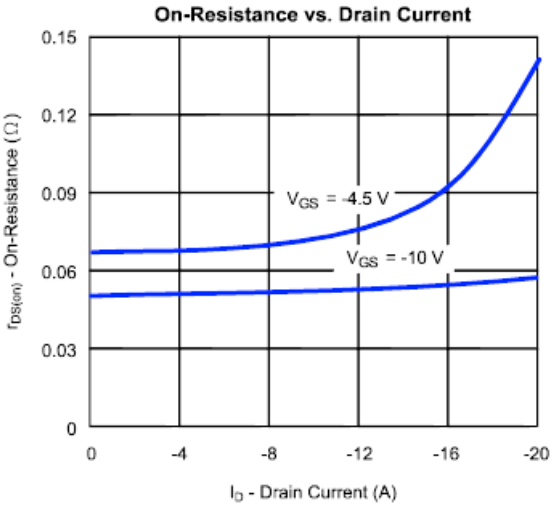
Notes: *The device mounted on 1in2 FR4 board with 2 oz copper

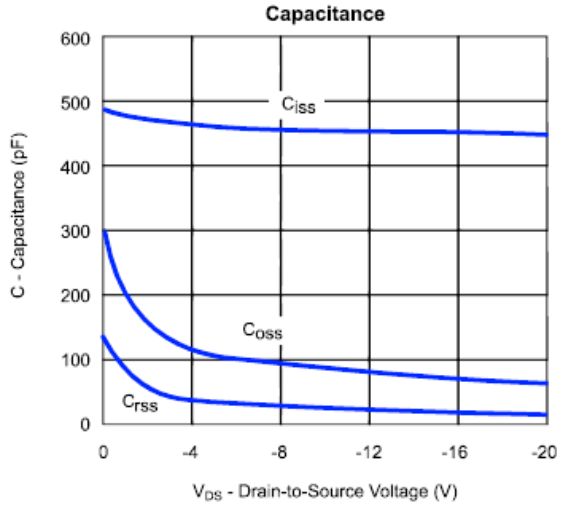
- **Electrical Characteristics** @T_A=25℃ unless otherwise Specified

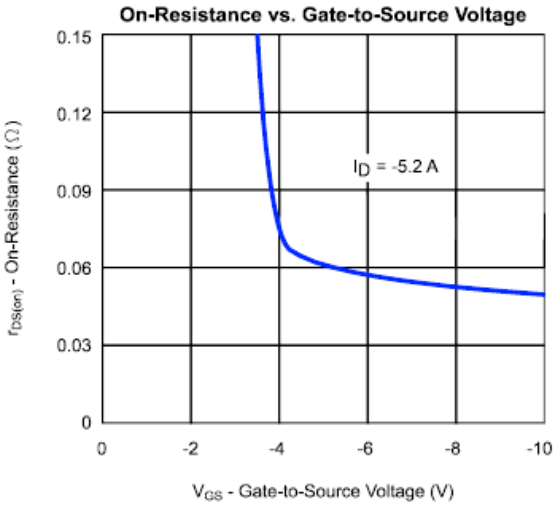
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} =V_{DS}, I_D= -250 A	-1	-1.4	-2	V
I_{GSS}	Gate Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	uA
		V_{DS} = -30V, V_{GS} = 0V,T_j=55	-	-	-25	
$I_{D(ON)}$	On-State Drain Current	V_{DS} = -5V, V_{GS} = -10V	-20	-	-	A
$R_{D(ON)}$	Drain-Source On-Resistance	V_{GS} = -10V, I_D= -5.3 A	-	50	60	mΩ
		V_{GS} = -4.5V, I_D= -4.2 A	-	69	90	
V_{SD}	Diode Forward Voltage	I_S= -1.7A, V_{GS} =0V	-	-0.8	-1.2	V
Dynamic						
R_g	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	-	3.5	-	Ω
C_{iss}	Input capacitance	V_{DS}=-15V, V_{GS}=-0V,f=1MHz	-	450	490	pF
C_{oss}	Output Capacitance		-	70	-	
C_{rss}	Reverse Transfer Capacitance		-	20	-	
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-5.3A	-	14	17	nC
Q_{gs}	Gate-Source Charge		-	4	-	
Q_{gd}	Gate-Drain Charge		-	3	-	
$t_{D(on)}$	Turn-On Delay Time	V_{DD}= -15V, R_L = 15Ω I_D = -1A, V_{GEN}=-10V R_G = 6Ω	-	27	33	ns
t_r	Turn-On Rise Time		-	11	15	
$t_{D(off)}$	Turn-Off Delay Time		-	40	52	
t_f	Turn-Off Fall Time		-	4	6	

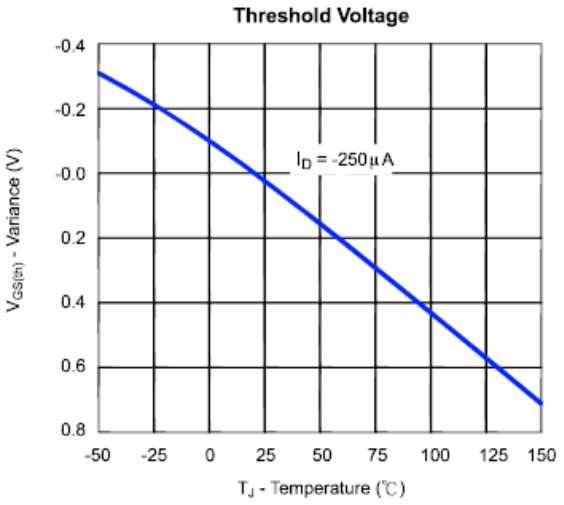
- **Typical Performance Characteristics (T_j=25)**

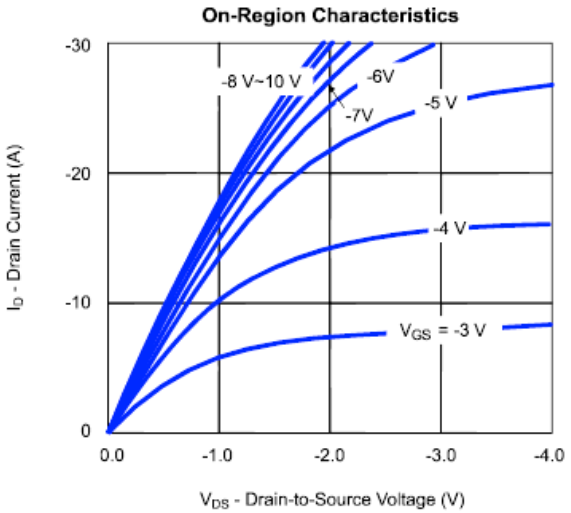




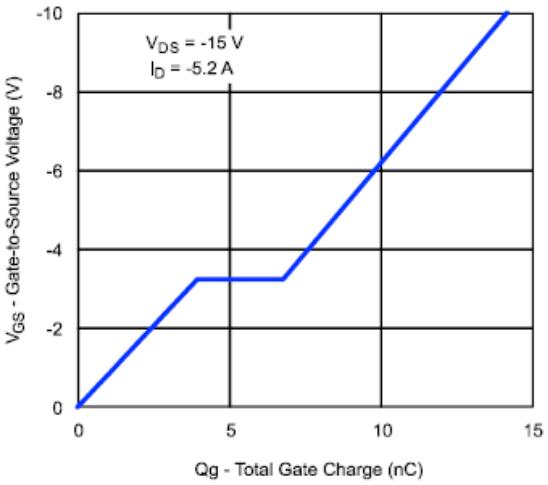




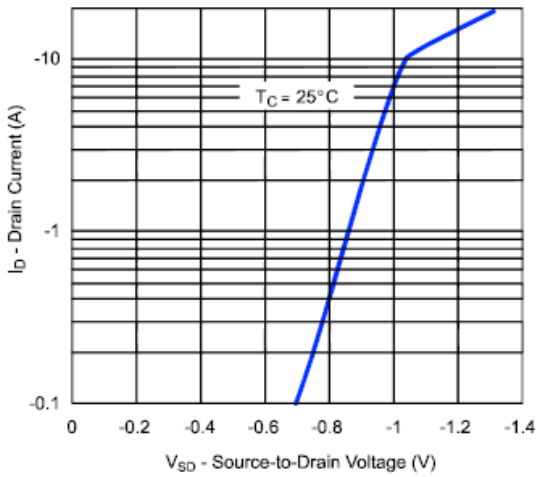




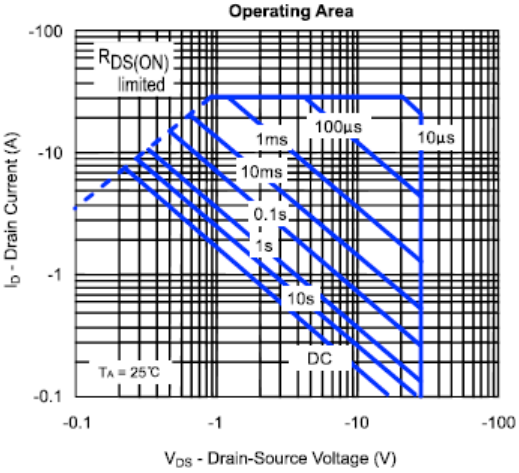
Gate Charge



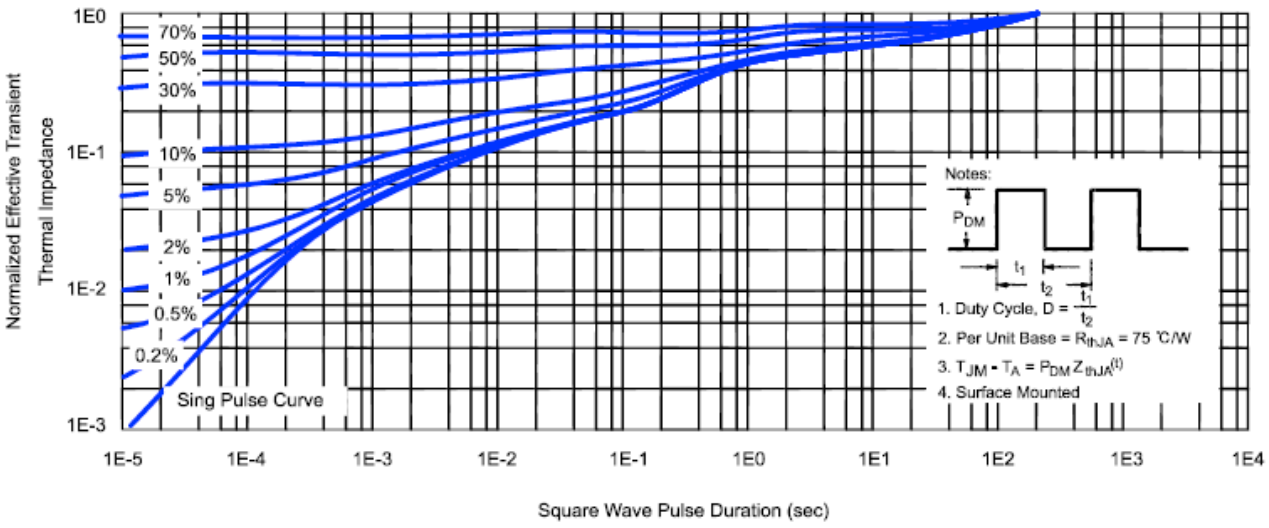
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area

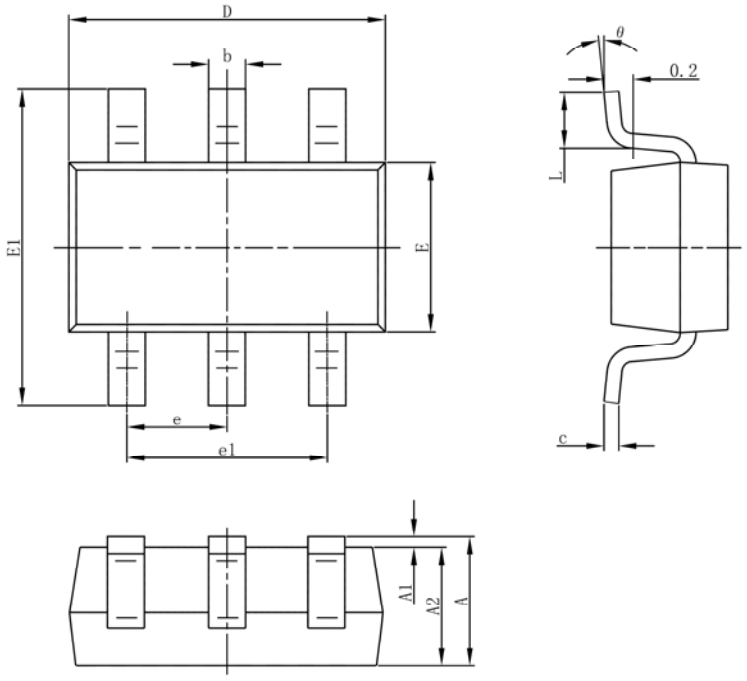


Normalized Thermal Transient Impedance, Junction-to-Ambient



- **Package Information**

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°