N-Channel Enhancement Mode Field Effect Transistor

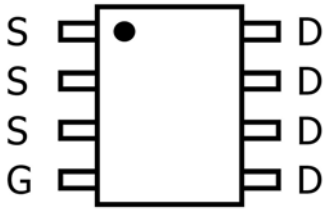
Features

- N-channel, normal leve
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC for target application
- Ideal for high-frequency switching and synchronous rectification

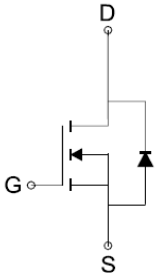
Product Summary

V_{DS}	V_{GS}	Test Conditions	$R_{DS(on)}$
60V	±20V	5A@VGS=10V	35mR
		4.5A@ VGS=4V5	40mR

Pin Configurations(TO252)



Top View



N-Channel MOSFET

Absolute Maximum Ratings TA=25°C unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	5 (1A) 20 (1B)	A
	Pulse	I_{DM}	60	
Total Power Dissipation (note1)		P_D	0.8 (1A) 25 (1B)	W
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes

1A、Surface Mounted on 1x1FR4 Board.

1B、Pulse width limited maximum junction temperature Pulse test: PW≤300 us duty cycle ≤2%

2、 The value of PD is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The value in any given application depends on the user's specific board design. The current rating is based on the DC thermal resistance rating and PCB layout: A. Minimum footprint; B. With additional heat sink.

3、 Repetitive rating, pulse width limited by junction temperature

Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter (note2)	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}= 0 V, I_D= 250 uA	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 60 V, V_{GS}= 0 V	--	--	1	uA
Gate–Body Leakage	I_{GSS}	V_{GS} = ± 20 V, V_{DS}= 0 V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}= V_{GS}, I_D= 250 uA	1	1.4	3	V
Static Drain–Source On–Resistance	$R_{DS(ON)}$	V_{GS}= 10 V, I_D= 5.0 A	--	35	41	mR
		V_{GS}= 4.5 V, I_D= 4.5 A	--	40	55	
Input Capacitance	C_{ISS}	V_{DS} = 10 V, V_{GS}= 0 V, F = 1MHz	--	1180	--	pF
Output Capacitance	C_{OSS}		--	170	--	
Reverse Transfer Capacitance	C_{RSS}		--	100	--	
Turn–On Delay Time	$T_{D(ON)}$	V_{GS}=10V, V_{DS}=30V, R_L=5.4R, R_{GEN}=3R, I_D=5.5A	--	--	25	nS
Turn–On Rise Time	T_R		--	--	70	
Turn–Off Delay Tim	$T_{D(OFF)}$		--	--	300	
Turn–Off Fall Time	T_F		--	--	150	
Diode Forward Voltage	V_{SD}	V_{GS}= 0 V, I_S= 2 A	0.5	0.77	1.0	V

1、 The value of PD is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The value in any given application depends on the user's specific board design. The current rating is based on the DC thermal resistance rating and PCB layout: A. Minimum footprint; B. With additional heat sink.

2、 Repetitive rating, pulse width limited by junction temperature

- **TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

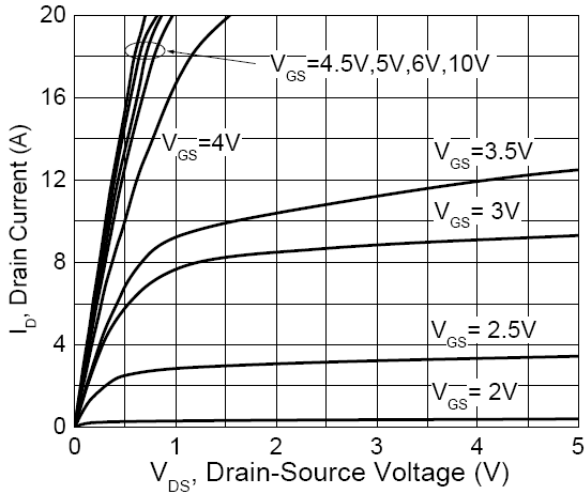


Figure 1. Output Characteristics

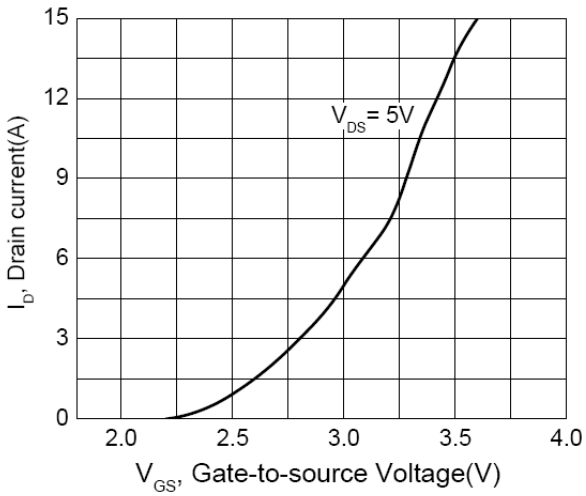


Figure 2. Transfer Characteristics

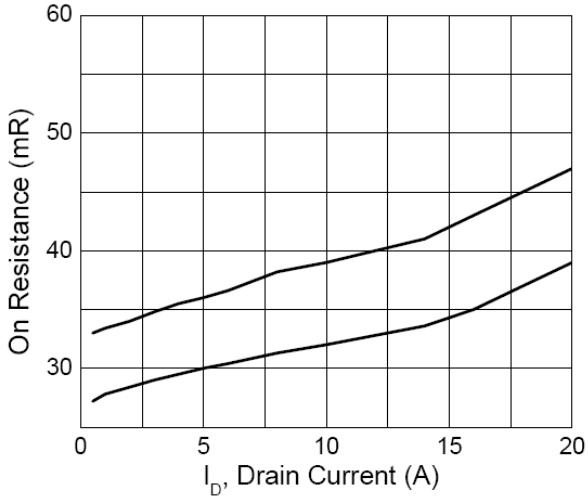


Figure 3. On-Resistance

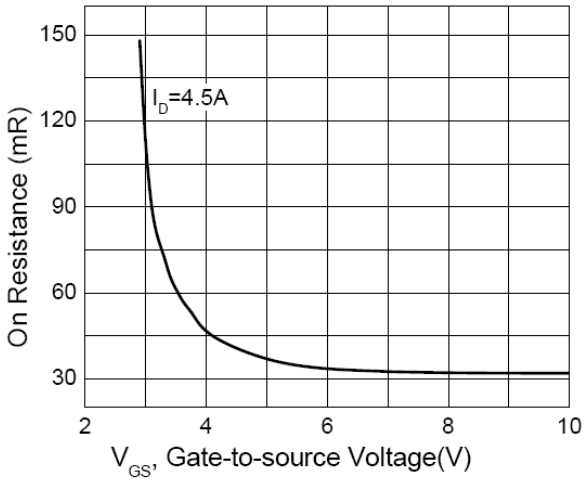


Figure 4. On-Resistance vs. Threshold Voltage

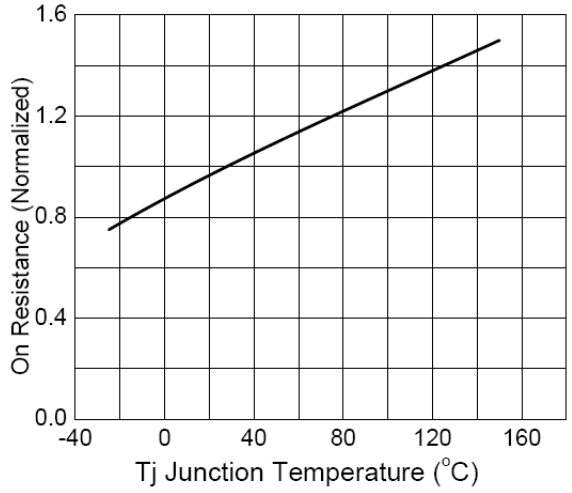


Figure 5 . On-Resistance vs. Temperature

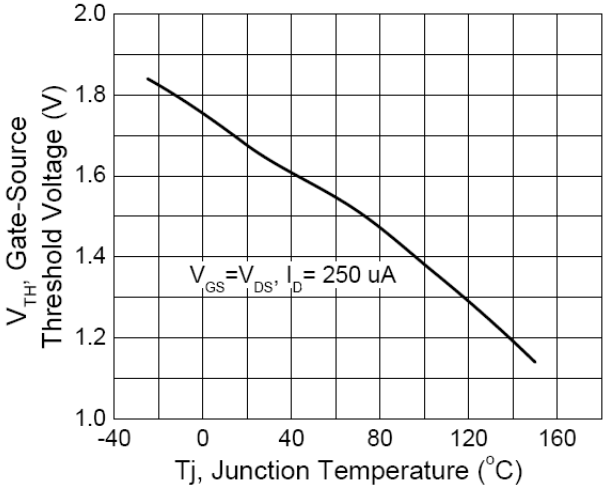
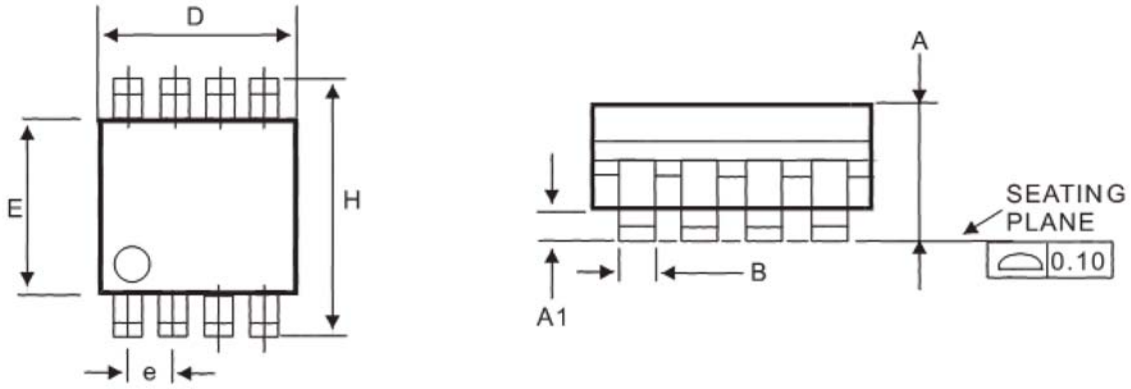
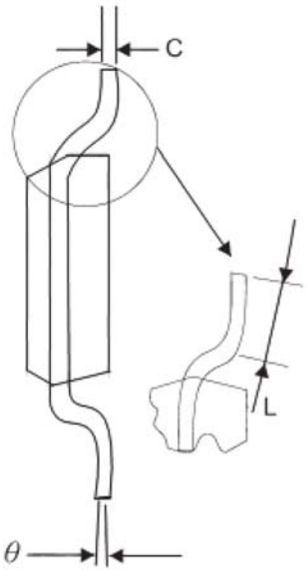


Figure 6. Gate Threshold Vs. Temperature

- **Package Information**

SOP-8 Package Outline





DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.