15V P-Channel MOSFET

● Features

-15V/±8V. 11A ,

$R_{DS(ON)}$ = 15mΩ @V_{GS} = -4.5V

$R_{DS(ON)}$ = 20mΩ @V_{GS} = -2.5V

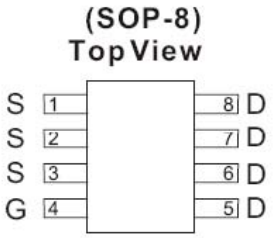
$R_{DS(ON)}$ = 27mΩ @V_{GS} = -1.8V

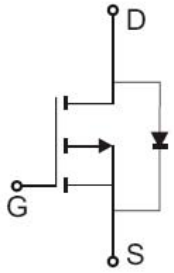
Lead Free Available (RoHS Compliant)

● General Description

The FS2235 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. this device is well suited for high current load applications.

● Pin Configuration





● Absolute Maximum Ratings T_A=25°C unless otherwise noted

Absolute Maximum Ratings (T_A=25 Unless Otherwise Noted)				
Parameter		Symbol	Limits	Units
Drain-Source Voltage		V_{DS}	-15	V
Gate-Source Voltage		V_{GS}	±8	V
MAX Continuous Drain Current		I_D	-11	A
Pulsed Drain Current1)		I_{DM}	-20	A
Maximum Power Dissipation	T_A=25	P_D	3	W
	T_A=70		2.1	
Operating Junction Temperature		T_J	-55 to 150	℃
Junction-to-Case Thermal Resistance		R_{JC}	30	/W
Junction-to-Ambient Thermal Resistance (PCB mounted) 2)		R_{JA}	50	/W

Notes: 1.Maximum DC current limited by the package 2.1-in2 2oz Cu PCB board

● Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC						
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=-250 A	-15			V
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = -4.5V, I_D = -11A		12	15	mΩ
		V_{GS} = -2.5V, I_D = -10A		17	20	
		V_{GS} =-1.8V, I_D = -6A		20	27	
$V_{GS(th)}$	Gate-Threshold Voltage	V_{GS} =VGS, I_D=-250 A	-0.5	-0.7	-0.9	V
I_{GSS}	Gate-Body Leakage	V_{GS} =+8V, V_{DS} = 0V			+100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -15V, V_{GS} = 0V			-1	A
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D =-11A		30		S
DYNAMIC						
Q_g	Total Gate Charge	V_{DS}=-15V, ID=-5A, V_{GS}=-8V		45		nC
Q_{gs}	Gate-Source Charge			10		
Q_{gd}	Gate-Drain Charge			8		
$t_{D(on)}$	Turn-On Delay Time	V_{DD}= -15V, R_L = 15 I_D = -1A, V_{GEN}=-8V R_G = 6		30		ns
t_r	Turn-On Rise Time			22		
$t_{D(off)}$	Turn-Off Delay Time			80		
t_f	Turn-Off Fall Time			34		

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

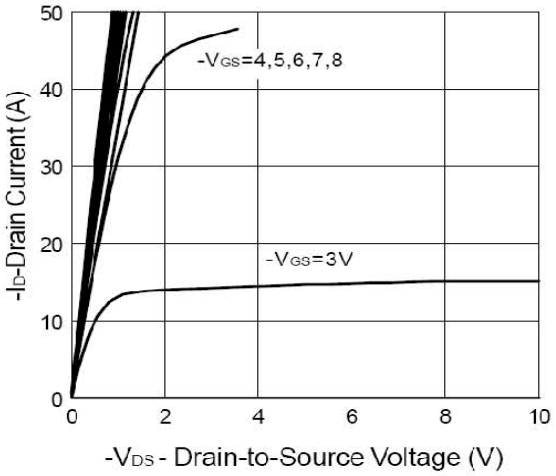
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

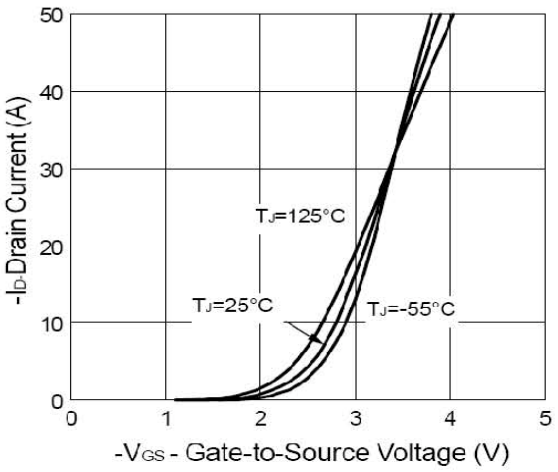
H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

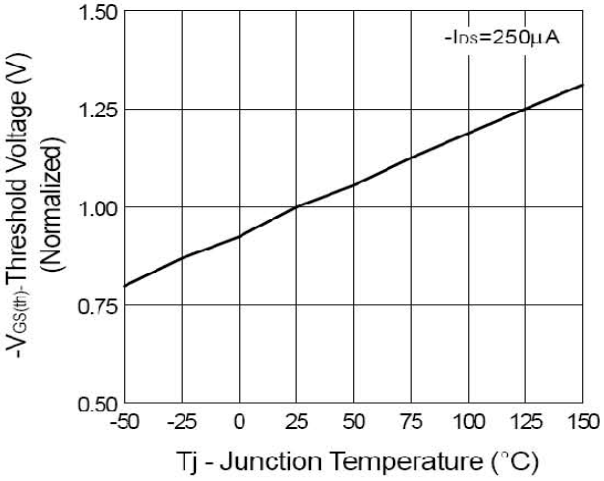
Output Characteristics



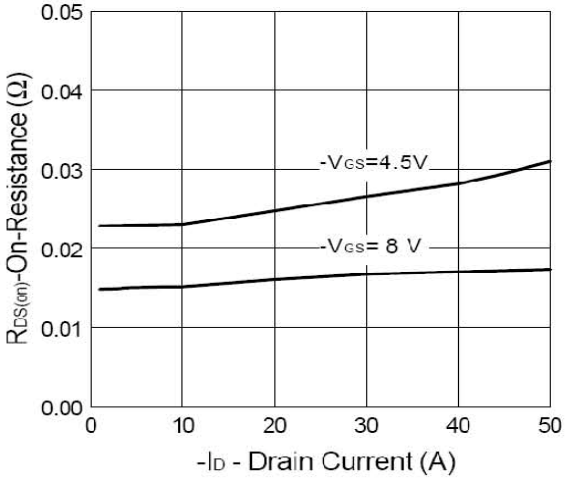
Transfer Characteristics



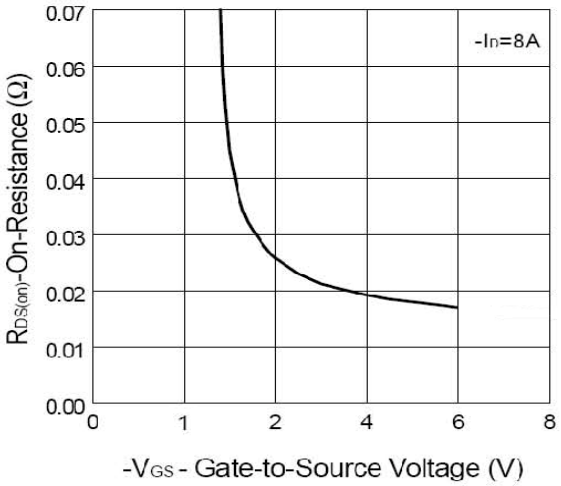
Threshold Voltage vs. Junction Temperature



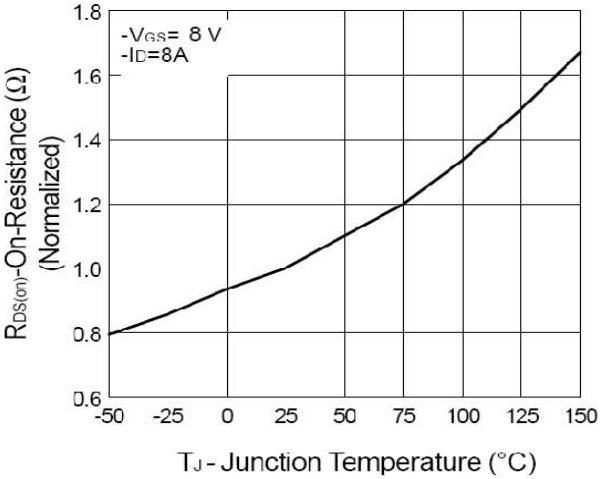
On-Resistance vs. Drain Current



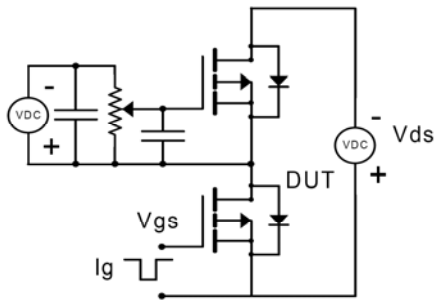
On-Resistance vs. Gate-to-Source Voltage

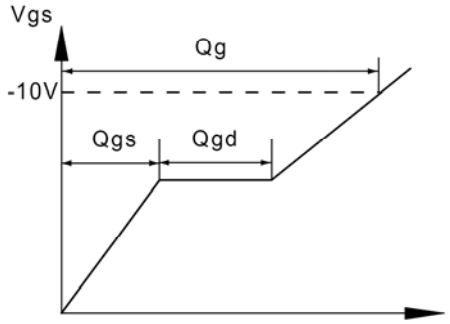


On-Resistance vs. Junction Temperature

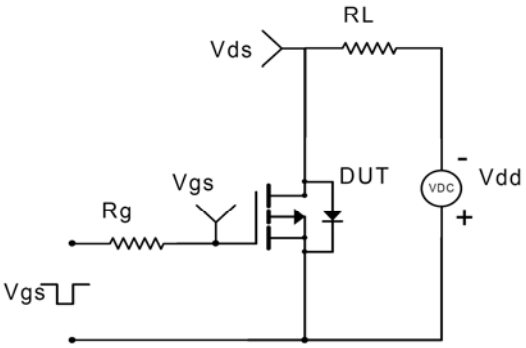


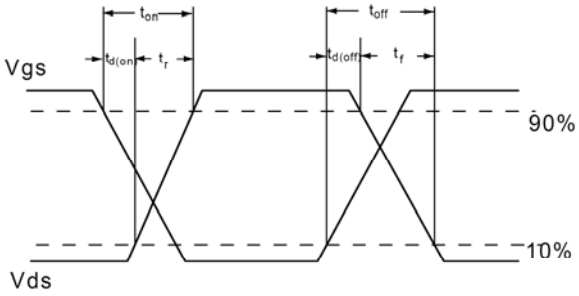
Gate Charge Test Circuit & Waveform



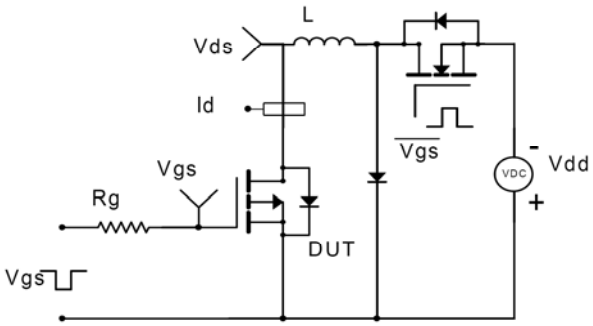


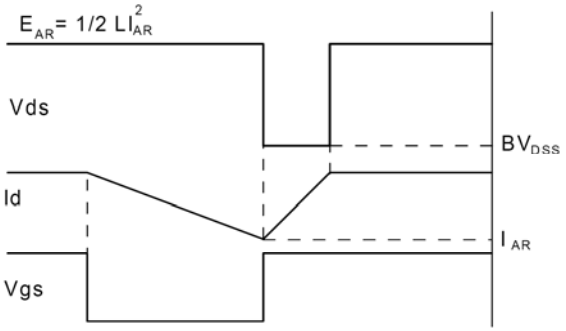
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms