30V P-Channel Enhancement Mode MOSFET

Features

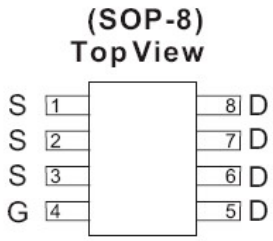
1.-30V/-5.3A, $RDS(ON)_{TYP}$=45mΩ @VGS=-10V

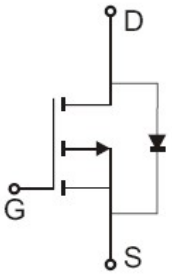
2.-30V/-4.2A, $RDS(ON)_{TYP}$=65mΩ@VGS=-4.5V

General Description

The FS9435 is the P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits,and low in-line power loss that are needed in a very small outline surface mount package.

Pin Configurations





Absolute Maximum Ratings @T_A=25℃ unless otherwise noted

Absolute Maximum Ratings (T_A=25 Unless Otherwise Noted)				
Parameter		Symbol	Limits	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	20	V
Continuous Drain Current		I_D	-5.3	A
Pulsed Drain Current[1)]		I_{DM}	-20	A
Maximum Power Dissipation	T_A=25	P_D	2.5	W
	T_A=70			
Operating Junction Temperature		T_J	-55 to 150	℃
Junction-to-Case Thermal Resistance		R_{JC}	30	/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]		R_{JA}	50	/W

Notes:

1.Maximum DC current limited by the package

2.1-in^2 2oz Cu PCB board

● **Electrical Characteristics** @T_A=25℃ unless otherwise noted

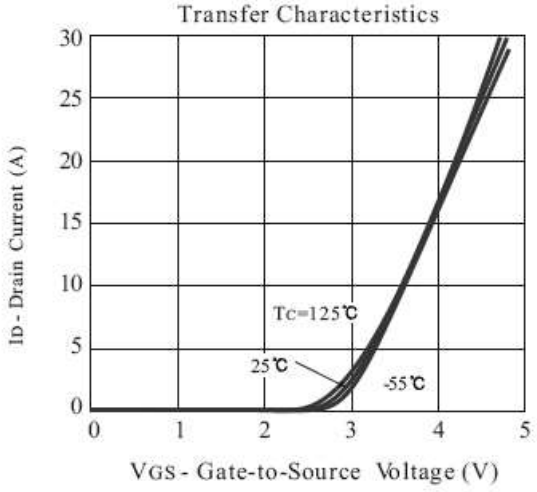
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static						
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=-250 A	-30			V
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} = -10V, I_D = -5.3A		45	55	mΩ
		V_{GS} =-4.5V, I_D = -4.2A		65	75	
$V_{GS(th)}$	Gate-Threshold Voltage	V_{GS} =VGS, I_D=-250 A	-1.0	-2.2	-3.0	V
I_{GSS}	Gate-Body Leakage	V_{GS} =+20V, V_{DS} = 0V			+100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V			-1	A
g_{FS}	Forward Transconductance	V_{DS} = -15V, I_D =-5.3A	4	7		S
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-15V, ID=-5.3A, V_{GS}=-10V		9.52		nC
Q_{gs}	Gate-Source Charge			3.43		
Q_{gd}	Gate-Drain Charge			1.71		
$t_{D(on)}$	Turn-On Delay Time	V_{DD}= -15V, R_L = 15 I_D = -1A, V_{GEN}=-10V R_G = 6		34.5		ns
t_r	Turn-On Rise Time			18.6		
$t_{D(off)}$	Turn-Off Delay Time			37.1		
t_f	Turn-Off Fall Time			3.1		

Notes:

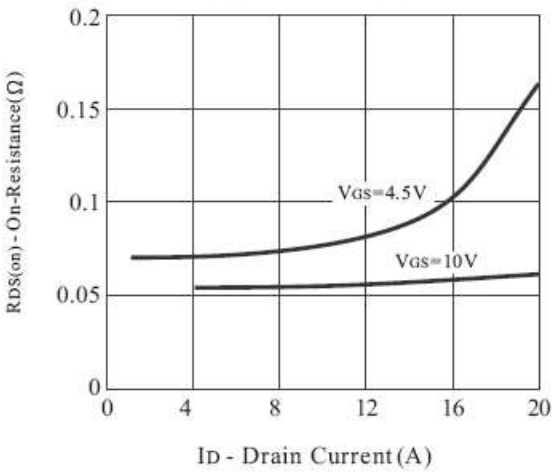
1. Pulse width limited by maximum junction temperature. Pulse test: $P_W \leqslant 300\ \mu s$, duty cycle≤2%.
2. For design AID only, not subject to production testing. Switching time is essentially independent of operating temperature.

- **Typical Performance Characteristics**

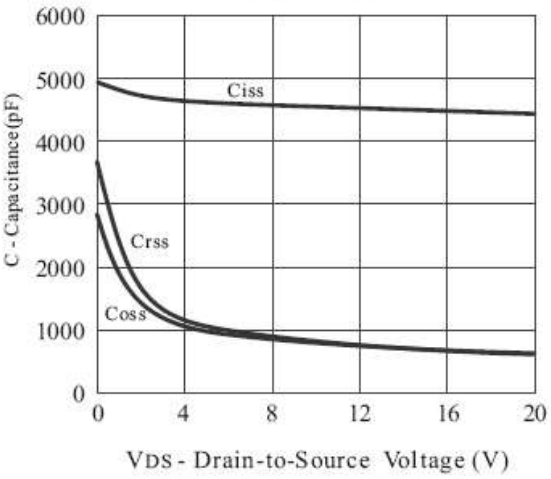
Transfer Characteristics



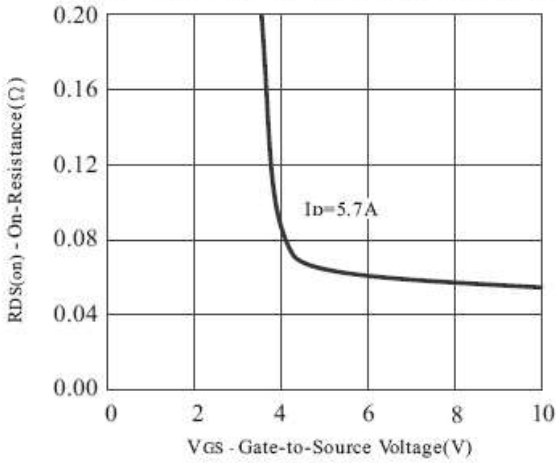
On- Resistance vs.Drain Current



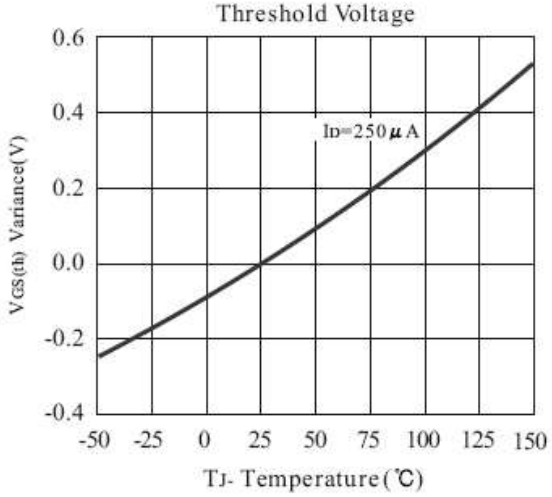
Capacitance



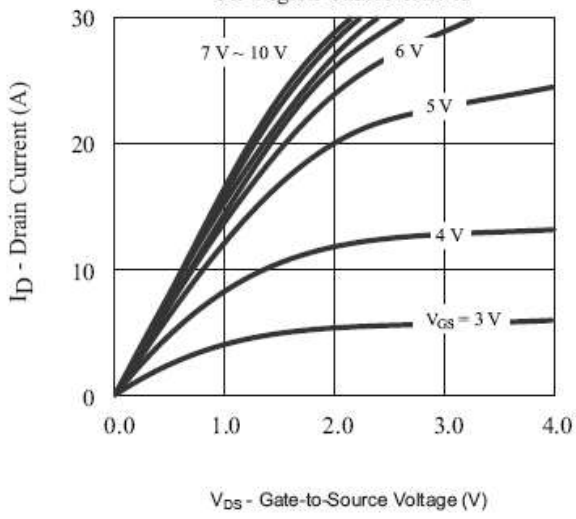
On- Resistance vs. Gate-to-Source Voltage



Threshold Voltage



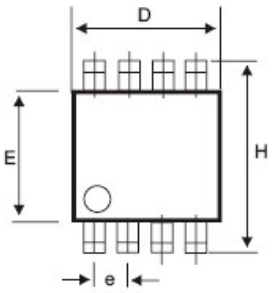
On-Region Characteristics

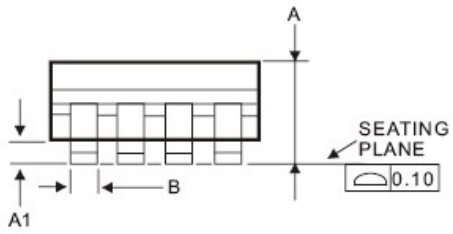


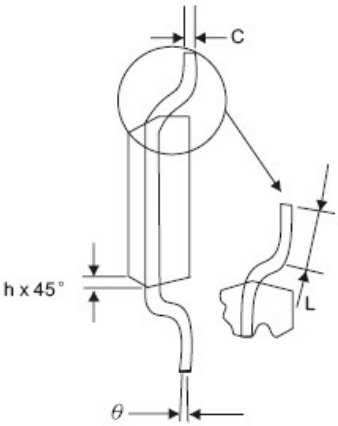
- **Package Information**

Physical Dimensions inches(millimeters) unless otherwise noted

SOP-8







DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

IMPORTANT NOTICE

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