



N-Channel 30-V (D-S) MOSFET

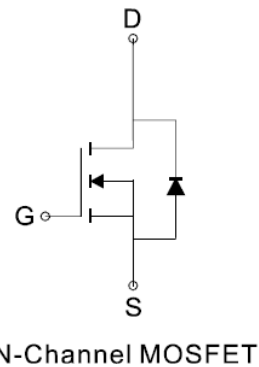
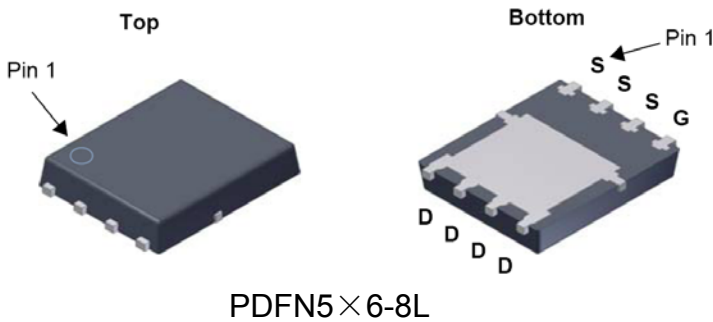
● **FEATURES**

- $R_{DS(ON)} \leq 0.87m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 1.89m\Omega @ V_{GS}=4.5V$
- high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

● **GENERAL DESCRIPTION**

The FS4472 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

● **PIN CONFIGURATION**



● **Absolute Maximum Ratings** ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDSS	30	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current ^{NOTE}	I_D	TA=25°C	A
		TA=100°C	
Pulsed Drain Current ^{NOTE}	I_{DM}	155	
Continuous Drain Current($T_J = 150^\circ C$)* ^{NOTE}	I_{DSM}	TA=25°C	A
		TA=70°C	
Maximum Power Dissipation*	PD	TA=25°C	W
		TA=70°C	
Operating Junction Temperature	T_J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	°C/W
Thermal Resistance-Junction to Lead*	$R_{\theta JL}$	24	

* The device mounted on 1in² FR4 board with 2 oz copper

NOTE: same as the second page



● **Electrical Characteristics** ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

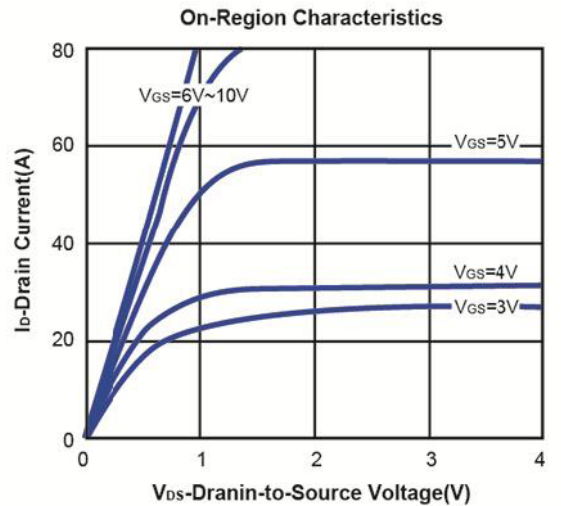
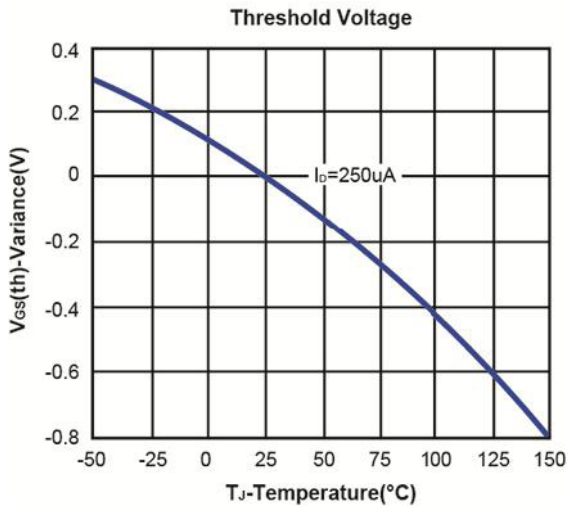
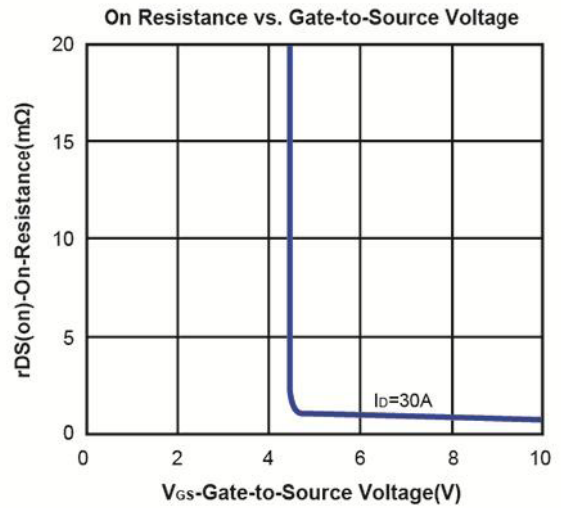
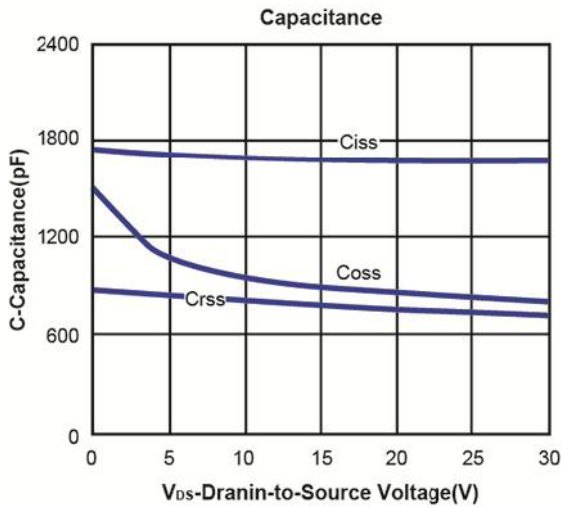
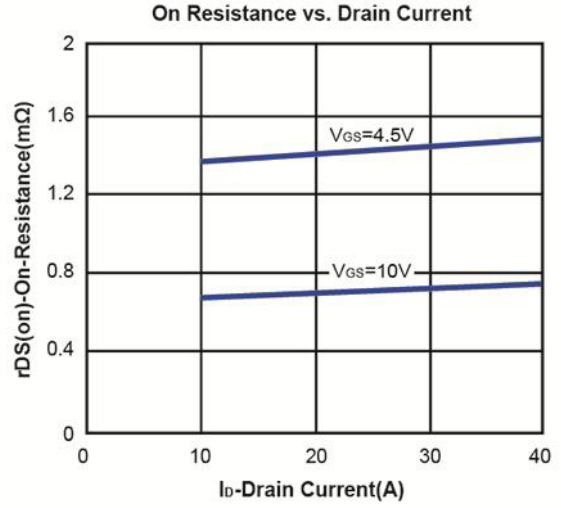
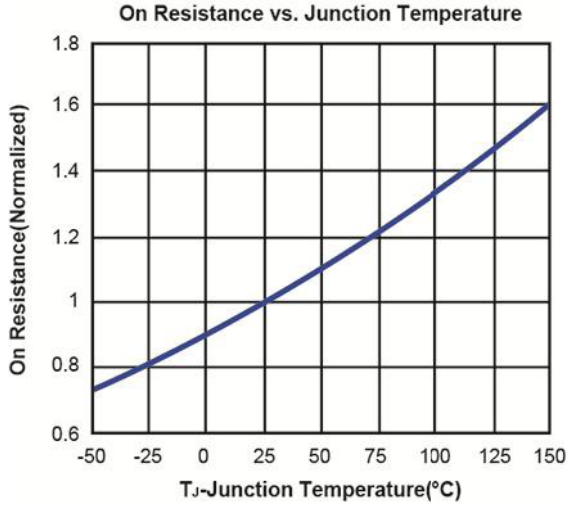
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250 μ A	30			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250 μ A	1.3		2.2	V
IGSS	Gate Leakage Current	VDS=0V, VGS= \pm 20V			\pm 100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V			1	μ A
RDS(ON)	Drain-Source On-State Resistance ^a	VGS=10V, ID= 30A		0.72	0.87	m Ω
		VGS=4.5V, ID= 30A		1.45	1.89	
VSD	Diode Forward Voltage	IS=10A, VGS=0V		0.73	1.1	V
DYNAMIC						
Qg	Total Gate Charge(10V)	VDS=15V, VGS=10V, ID=30A		209		nC
Qg	Total Gate Charge(4.5V)	VDS=15V, VGS=4.5V, ID=30A		106		
Qgs	Gate-Source Charge			40		
Qgd	Gate-Drain Charge			51		
Ciss	Input capacitance	VDS=15V, VGS=0V, f=1.0MHz		1670		pF
Coss	Output Capacitance			880		
Crss	Reverse Transfer Capacitance			760		
Rg	Gate-Resistance	VDS=0V, VGS=0V, f=1MHz		1.2		Ω
td(on)	Turn-On Delay Time	VDD=15V, RL =15 Ω ID=1A, VGEN=4.5V RG=3 Ω		80		ns
tr	Turn-On Rise Time			75		
td(off)	Turn-Off Delay Time			141		
tf	Turn-Off Fall Time			68		

Note:

- a: Pulse test: pulse width \leq 300 μ s, duty cycle \leq 2%
- b: FORSEMI reserves the right to improve product design, functions and reliability without notice.
- c. Single pulse width limited by junction temperature $T_J(\text{MAX})=150^{\circ}\text{C}$.
- d. The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.
- e. The static characteristics in Figures 1 to 6 are obtained using $<$ 300ms pulses, duty cycle 0.5% max.
- f. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX})=150^{\circ}\text{C}$. The SOA curve provides a single pulse rating.
- g. The maximum current rating is package limited.
- h. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$.

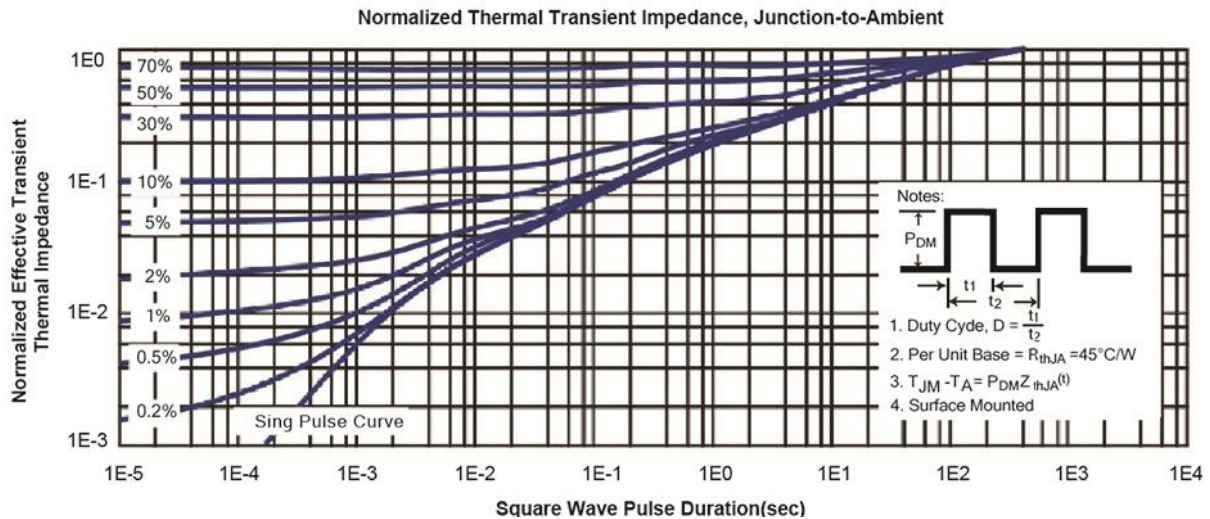
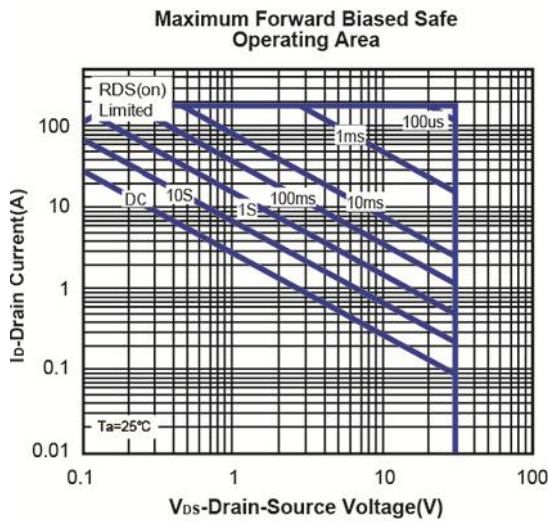
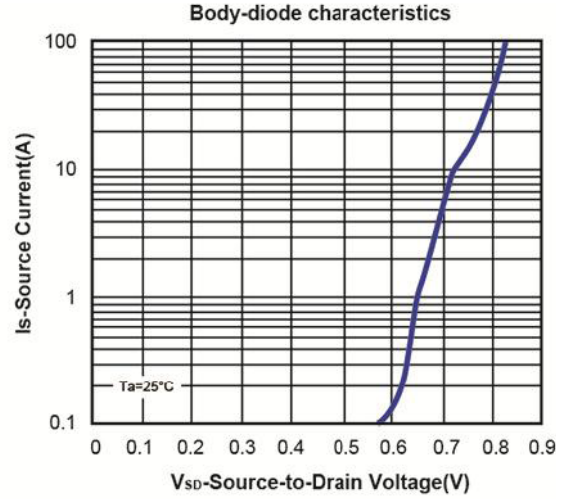
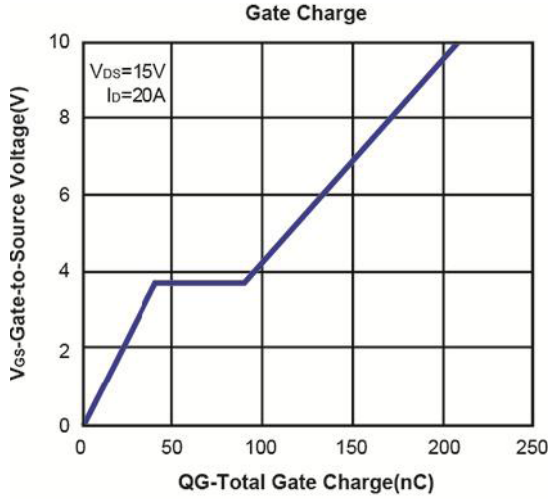


● Typical Characteristics



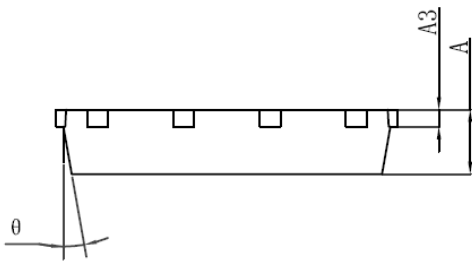
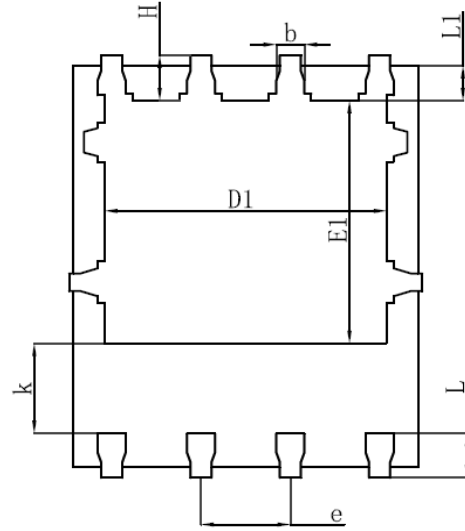
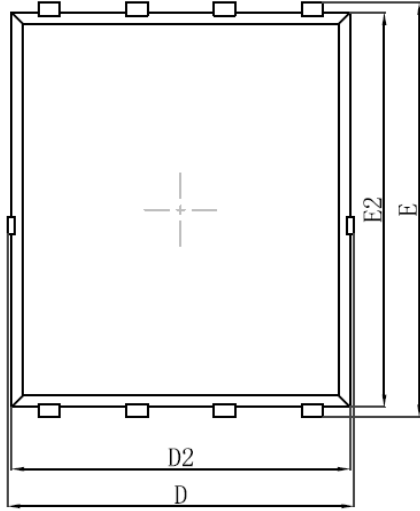


TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS





● PACKAGE PDFN5×6-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°