Dual N-Channel Power MOSFET

FEATURES

$$\begin{split} R_{DS(ON)} & \leq 16 m \quad @V_{GS} = 10V \\ R_{DS(ON)} & \leq 20 m \quad @V_{GS} = 4.5V \end{split}$$

Super high density cell design for extremely low $R_{\text{DS(ON)}}$ Exceptional on-resistance and maximum DC current capability

APPLICATIONS

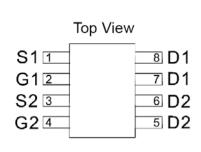
Power Management in Note book
Portable Equipment
Battery Powered System
DC/DC Converter
Load Switch
DSC
LCD Display inverter

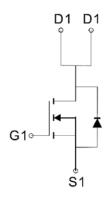
GENERAL DESCRIPTION

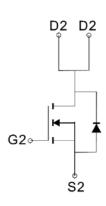
The FS4970 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

• PIN CONFIGURATION (SOP8)

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Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

| Parameter Drain-Source Voltage | | Symbol | Maximum | Units | |
|--|----------------------|-----------------------------------|------------|------------|--|
| | | V _{DS} | 30 | V | |
| Gate-Source Voltage | | V_{GS} | ±20 | V | |
| Continuous Drain Current | T _A =25°C | | 10 | A | |
| | T _A =70°C | I _D | 8.5 | | |
| Pulsed Drain Current ^C | | I _{DM} | 32 | 7 | |
| Power Dissipation ^B | T _A =25°C | | 2 | W | |
| Power Dissipation | T _A =70°C | P_D | 1.5 | | |
| Junction and Storage Temperature Range | | T _J , T _{STG} | -55 to 150 | $^{\circ}$ | |

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■ **Electrical Characteristics** (T_A=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Тур | Max | Units | | | |
|---------------------|--------------------------------------|---|-----|------|-------|-------|--|--|--|
| STATIC PARAMETERS | | | | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250uA, V _{GS} =0V | 30 | | | V | | | |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =24V, V _{GS} =0V | | | 1 | uA | | | |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} =±20V | | | ± 0.1 | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250uA | 1 | 1.4 | 2 | V | | | |
| R _{DS(ON)} | Obetic Design Courses On Designation | V _{GS} =10V, I _D =10A | | 13 | 16 | mΩ | | | |
| | Static Drain-Source On-Resistance | V_{GS} =4.5V, I_D =8A | | 16.5 | 20 | | | | |
| V_{SD} | Diode Forward Voltage | I _S =2.3A,V _{GS} =0V | | 0.8 | 1.2 | V | | | |
| DYNAMIC | PARAMETERS | | | | l . | | | | |
| C _{iss} | Input Capacitance | | | 680 | | pF | | | |
| Coss | Output Capacitance | V _{GS} =0V, V _{DS} =10V, f=1MHz | | 120 | | | | | |
| C _{rss} | Reverse Transfer Capacitance | | | 32 | | | | | |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | | 1 | | Ω | | | |
| SWITCHI | NG PARAMETERS | | | | | | | | |
| Qg | Total Gate Charge | | | 9.5 | | | | | |
| Q _{gs} | Gate Source Charge | V _{GS} =4.5V, V _{DS} =10V, I _D =8.2A | | 3.8 | | | | | |
| Q_{gd} | Gate Drain Charge | | | 3.2 | | | | | |
| t _{D(on)} | Turn-On DelayTime | | | 12 | | ns ns | | | |
| tr | Turn-On Rise Time | V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V | | 9 | | | | | |
| $t_{\text{D(off)}}$ | Turn-Off DelayTime | $R_G=6\Omega$ | | 42 | | | | | |
| t _f | Turn-Off Fall Time | | | 5 | | | | | |

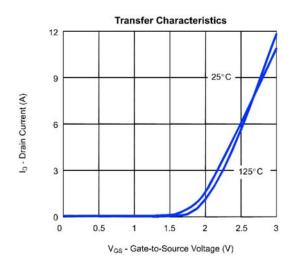
A. The value of $R_{\theta,JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

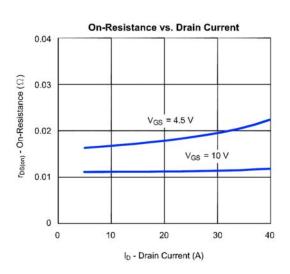
- B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using≤10s junction-to-ambient thermal resistance.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.
- D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300us pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$ =150°C. The SOA curve provides a single pulse rating.

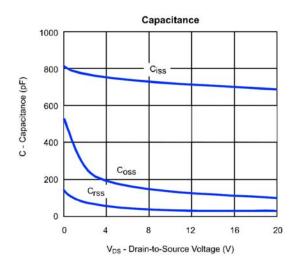
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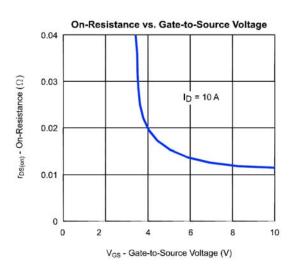


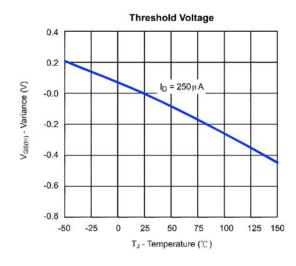
• TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

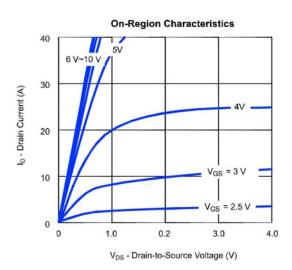










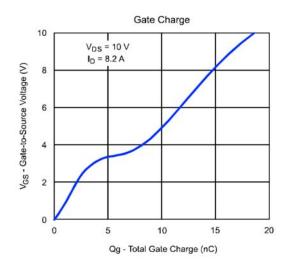


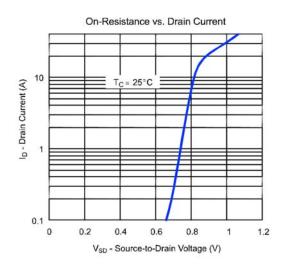
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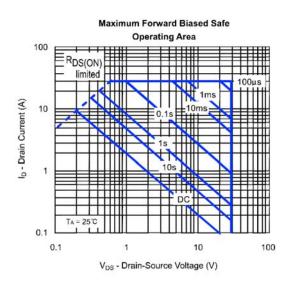
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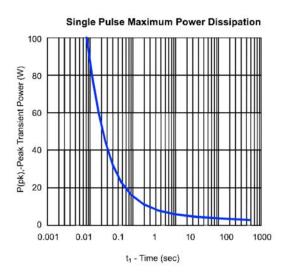


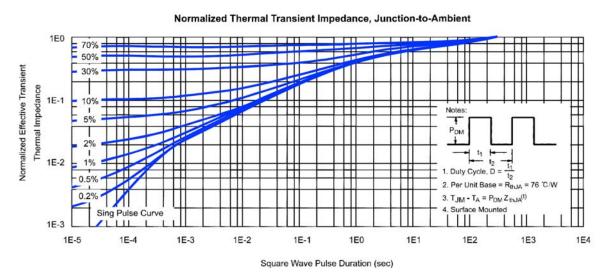
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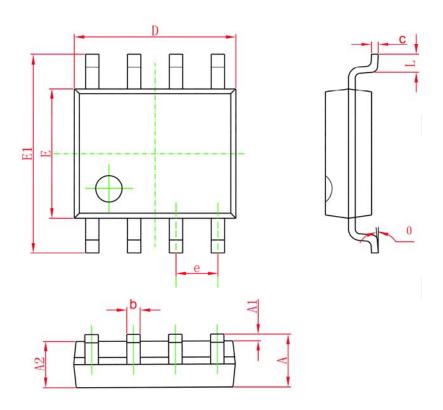


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Package Information

SOP8 PACKAGE OUTLINE DIMENSIONS



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | | |
|--------|---------------------------|-------|----------------------|-------|--|
| | Min | Max | Min | Max | |
| А | 1.350 | 1.750 | 0.053 | 0.069 | |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 | |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 | |
| b | 0.330 | 0.510 | 0.013 | 0.020 | |
| С | 0.170 | 0.250 | 0.006 | 0.010 | |
| D | 4.700 | 5.100 | 0.185 | 0.200 | |
| Е | 3.800 | 4.000 | 0.150 | 0.157 | |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 | |
| е | 1.270(BSC) | | 0.050(BSC) | | |
| L | 0.400 | 1.270 | 0.016 | 0.050 | |
| θ | 0° | 8° | 0° | 8° | |

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