Dual N-Channel 100V（D-S）MOSFET

Features

- $R_{DS(ON)}$ < 80mΩ@V_{GS} = 10V
- $R_{DS(ON)}$ < 98mΩ@V_{GS} = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

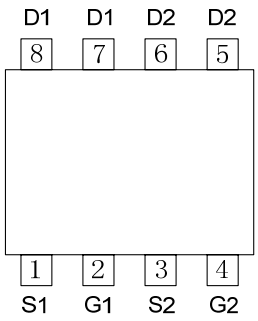
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

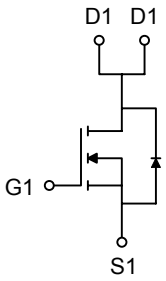
GENERAL DESCRIPTION

The FS4980 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

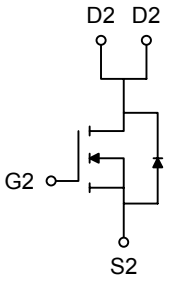
Pin Configuration

SOP8 (TopView)





N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings @ T_A = 25°C unless otherwise specified

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current		I_D	4	A
Pulsed Drain Current		I_{DM}	16	A
Maximum Power Dissipation	T_A=25°C	P_D	2	W
	T_A=70°C		1.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62.5	℃/W

Notes：

a. mounted on a 1in2 FR-4 board with 2oz. Copper in a still air environment at 25°C，the current rating is based on the DC（<10s）test conditions , for each single die.

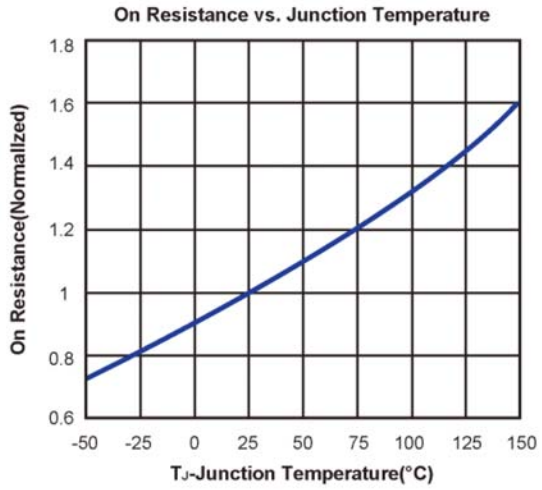
b. Pulse Test：Pulse Width < 300 μs, Duty Cycle < 2%.

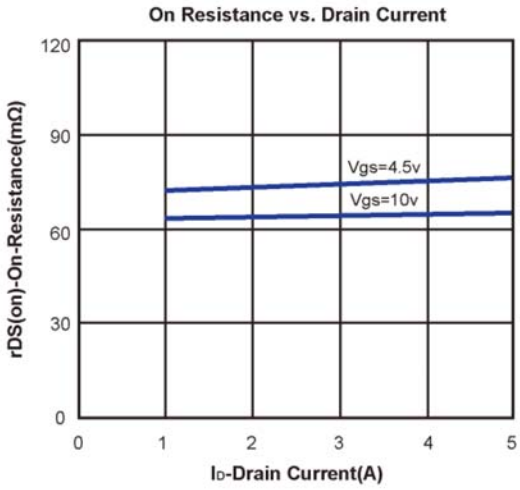
- **Electrical Characteristics** @ T_A = 25°C unless otherwise specified

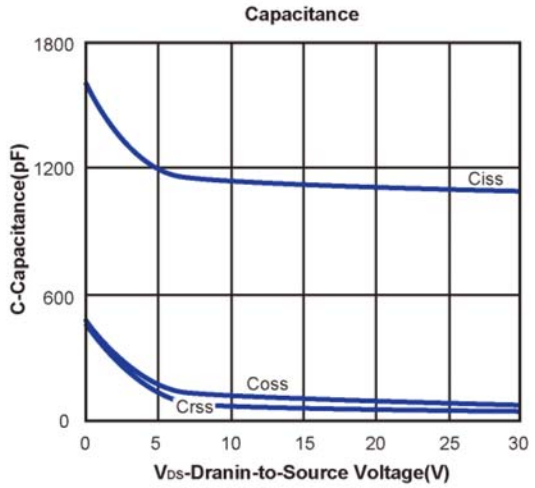
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=VGS, I_D=250μA	1		2.5	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=± 20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance(1)	V_{GS}=10V, I_D= 4A		65	80	mΩ
		V_{GS}=4.5V, I_D= 3.2A		75	98	
G_{FS}	Forward Transconductance	V_{DS}=10V, I_D=6.0A	7	13		S
V_{SD}	Diode Forward Voltage	I_S=12A, V_{GS}=0V			1.3	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DS}=80V, V_{GS}=5V, I_D=4A		17.5		nC
Q_{gs}	Gate-Source Charge			10		
Q_{gd}	Gate-Drain Charge			5.5		
$t_{d(on)}$	Turn-On Time	V_{DD}=50V,R_L=12.5Ω,I_D=4A, V_{GEN}=5V, R_G=4.7Ω		27.5		nS
t_r	Turn-On Rise Time			90		
$t_{d(off)}$	Turn-Off Delay Time			35		
t_f	Turn-On Fall Time			11		
C_{iss}	Input capacitance	V_{DS}=10V, V_{GS}=0V, f=1.0MHz		1100		pF
C_{oss}	Output Capacitance			72		
C_{rss}	Reverse Transfer Capacitance			45		

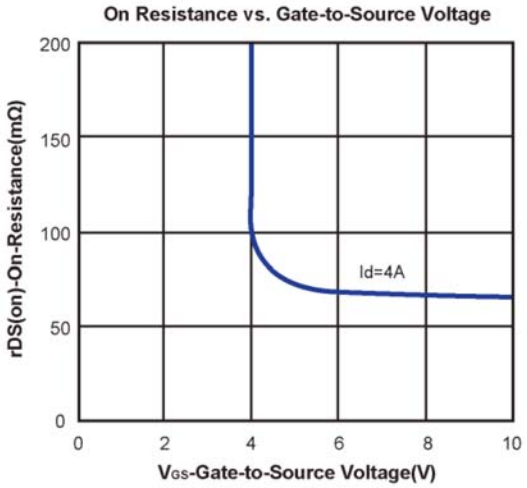
Notes: (1) Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

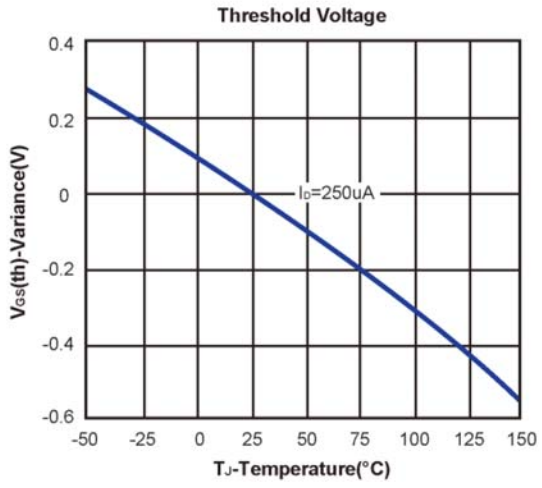
- **Typical Performance Characteristics**

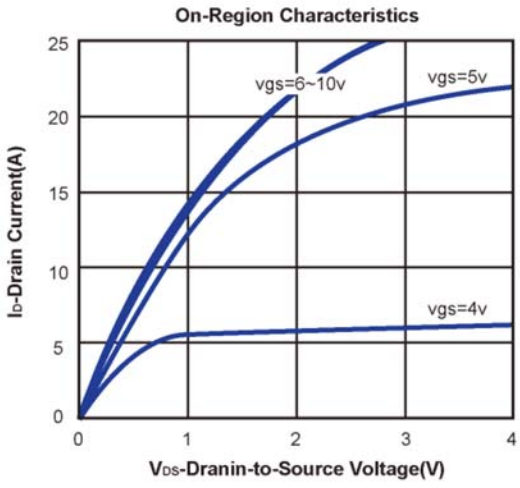






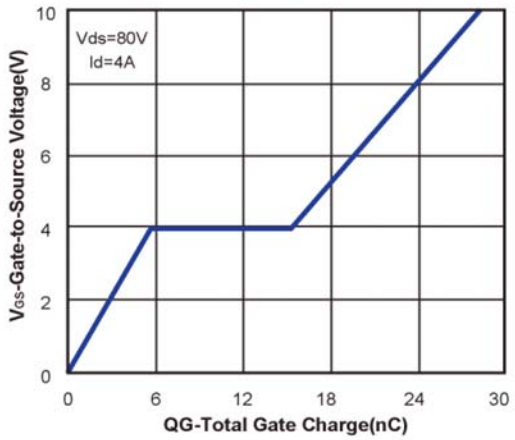




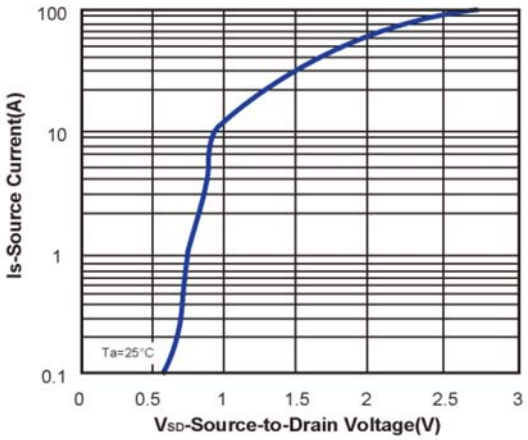


- **Typical Performance Characteristics**

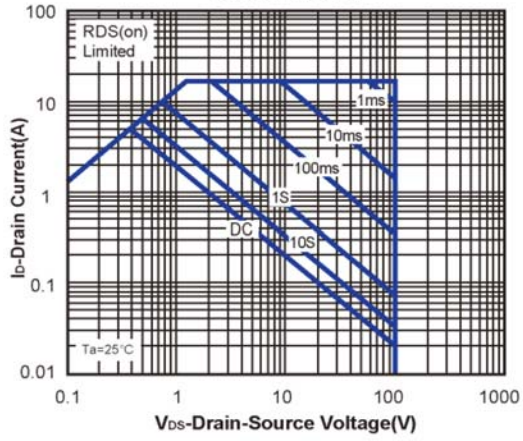
Gate Charge



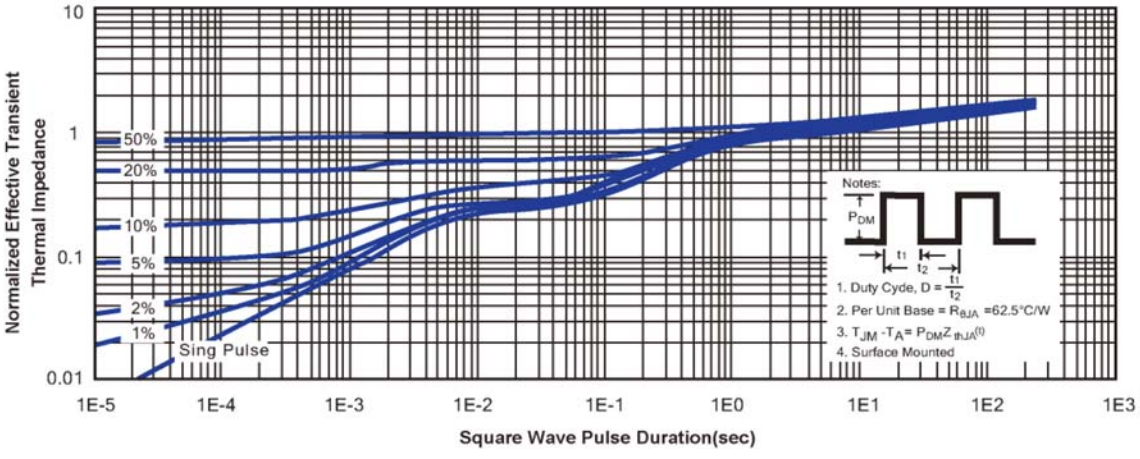
Body-diode characteristics



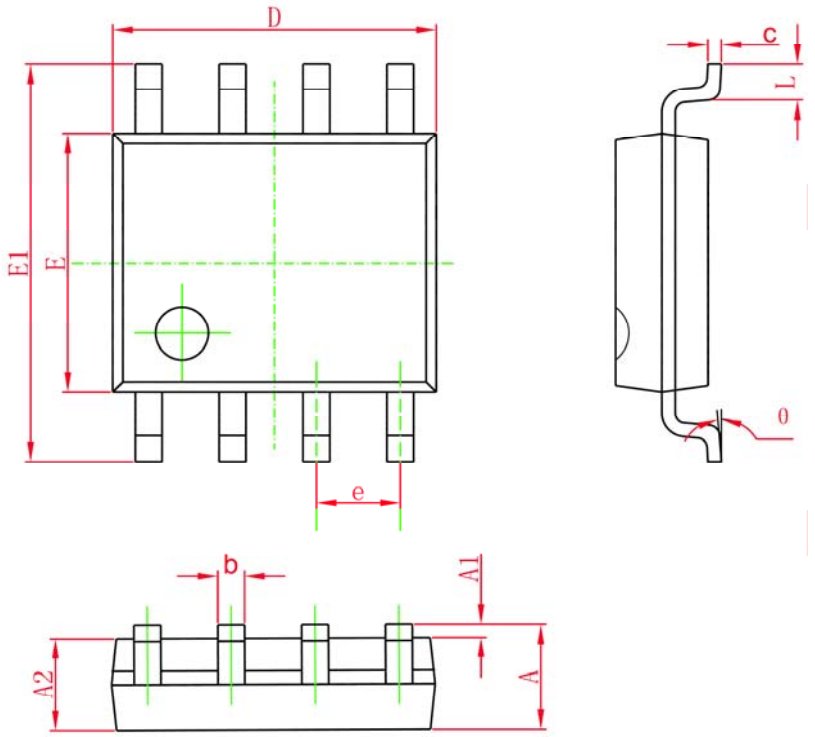
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



- **Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°