



DUAL N-CANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

● Features

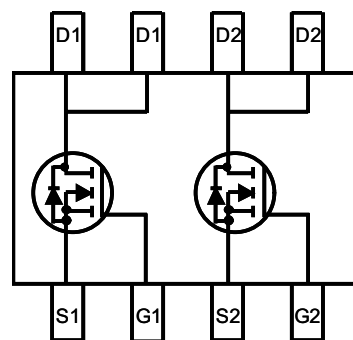
- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance
- High Power and Current handing capability
- Fully Characterized Avalanche Voltage and Current

● General Description

- Case: SOP8
- Case Material: Molded Plastic. UL Flammability Classification
- Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208

● Pin configurations

See Diagram below



● Maximum Ratings @ T_A = 25°C unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V _{DSS}	20	V
Gate-Source Voltage		V _{GSS}	±12	
Drain Current (Note 1)	Continuous	I _D	3.7	A
	Pulsed		6	
Total Power Dissipation (Note 1)		P _D	0.69	W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Note: 1. Mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch, for each singlate die, the P_D is 75%.



● **Electrical Characteristics** @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$	--	--	1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$	--	--	± 100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6	--	--	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 6A$	--	25	50	m Ω
		$V_{GS} = 2.5V, I_D = 5.2A$	--	34	65	
Forward Transconductance	g_{FS}	$V_{DS} = 10V, I_D = 6A$	--	5	--	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0V$ $f = 1.0MHz$	--	562	--	pF
Output Capacitance	C_{oss}		--	79	--	
Reverse Transfer Capacitance	C_{rss}		--	73	--	
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 6A,$ $V_{GS} = 4.5V$	--	4.86	--	nC
Gate-Source Charge	Q_{gs}		--	0.92	--	
Gate-Drain	Q_{gd}		--	1.4	--	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 10V, I_D = 1A,$	--	18	--	ns
Turn-Off Delay Time	$t_{D(OFF)}$	$V_{GEN} = 4.5V, R_G = 6\Omega$	--	25	--	

Note: 2. Short duration test pulse used to minimize self-heating effect.



● Typical Performance Characteristics

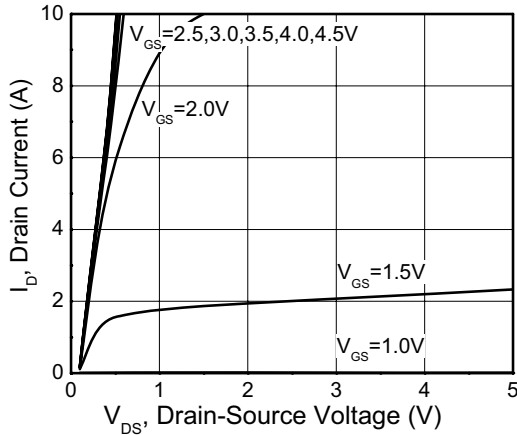


Figure 1. Output Characteristics

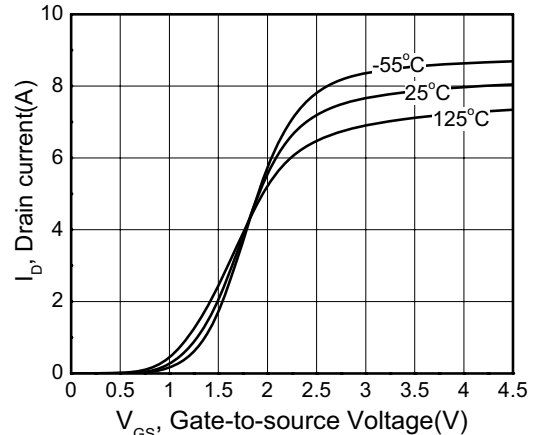


Figure 2. Transfer Characteristics

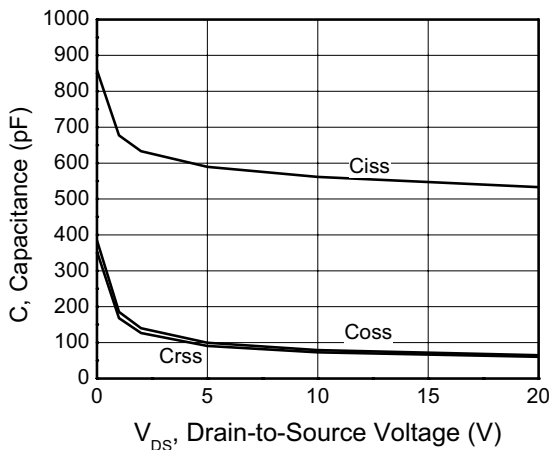


Figure 3. Capacitance

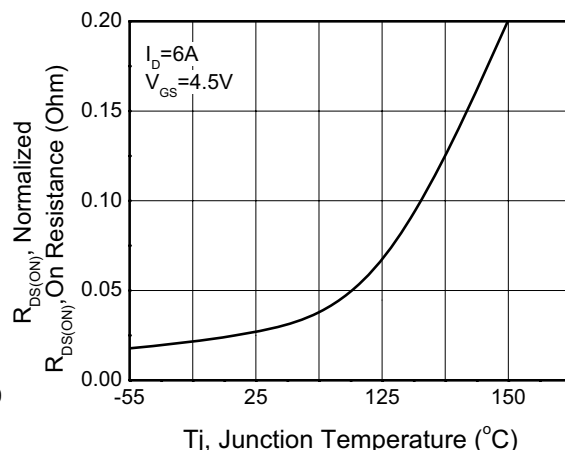


Figure 4. On Resistance Vs. Temperature

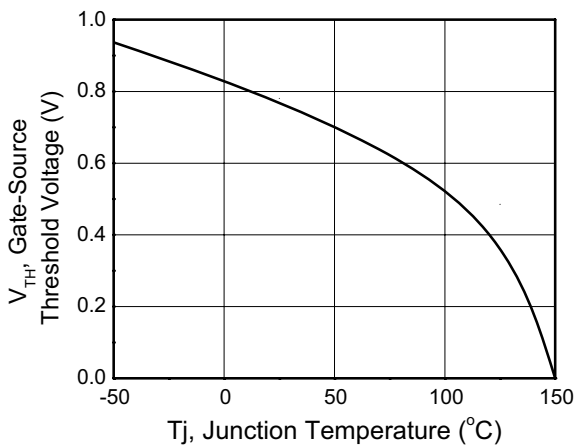


Figure 5. Gate Threshold Vs. Temperature

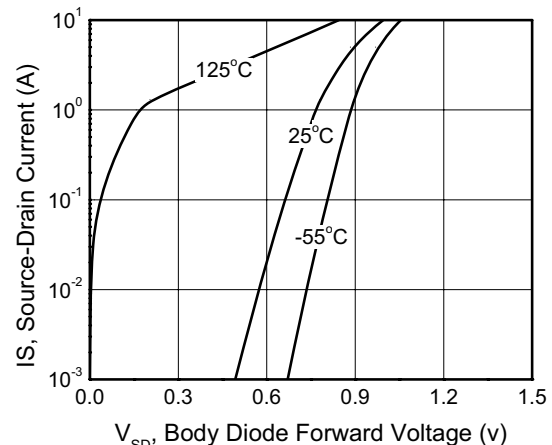
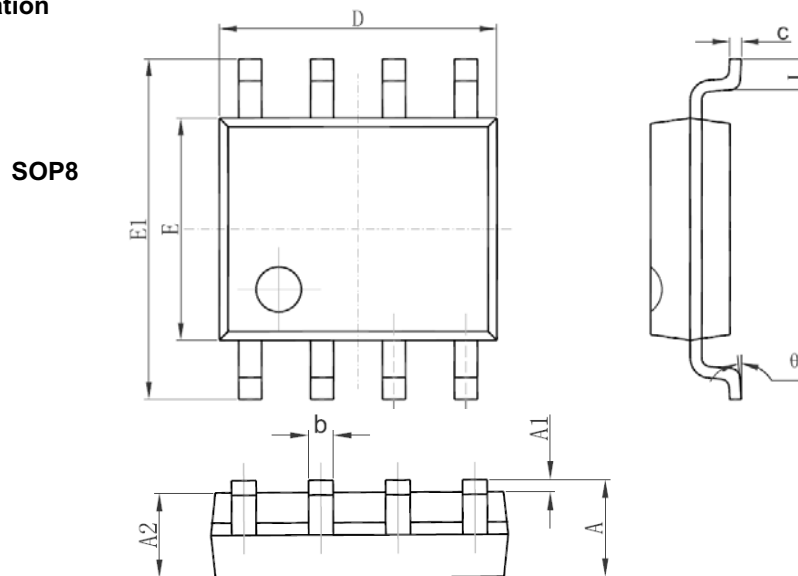


Figure 6. Body Diode Forward Voltage Vs. Source Current



● Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°