



## 40V P-Channel Enhancement Mode MOSFET

- **Features**

- -40V/-10A,  $R_{DS(ON)}=38m@V_{GS}=-10V$
- -40V/ -8A,  $R_{DS(ON)}=54m @V_{GS}= -4.5V$
- Super high density cell design for extremely
- low  $R_{DS(ON)}$
- TO-252-2L package design

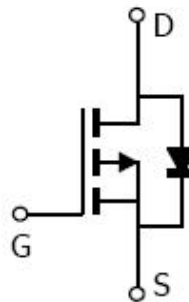
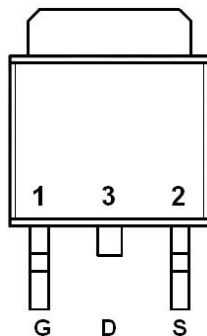
- **Applications**

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter
- LED Display
- Load Switch
- CCFL Inverter

- **General Description**

LSP52H, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

- **Pin Description ( TO-252-2L )**





● **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

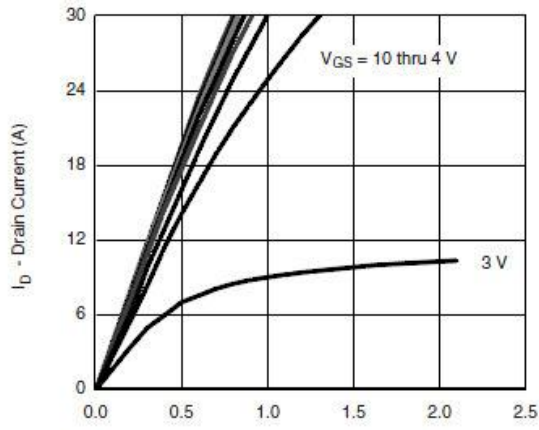
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		$V_{DSS}$	-40	V
Gate –Source Voltage		$V_{GSS}$	$\pm 20$	
Continuous Drain Current( $T_J=150^{\circ}\text{C}$ )	$T_A=25^{\circ}\text{C}$	$I_D$	-22	A
	$T_A=70^{\circ}\text{C}$		-16	
Pulsed Drain Current		$I_{DM}$	-30	
Continuous Source-Drain Diode Current		$I_S$	-8	
Single Pulse Avalanche Current	$L = 0.1 \text{ mH}$	$I_{AS}$	-30	
Avalanche Energy		$E_{AS}$	35	mJ
Power Dissipation	$T_A=25^{\circ}\text{C}$	$P_D$	40	W
	$T_A=70^{\circ}\text{C}$		15	
Operating Junction Temperature		$T_J$	150	$^{\circ}\text{C}$
Storage Temperature Range		$T_{STG}$	-55/150	
Thermal Resistance-Junction to Ambient		$R_{JA}$	62.5	$^{\circ}\text{C}/\text{W}$

● **Electrical Characteristics**( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

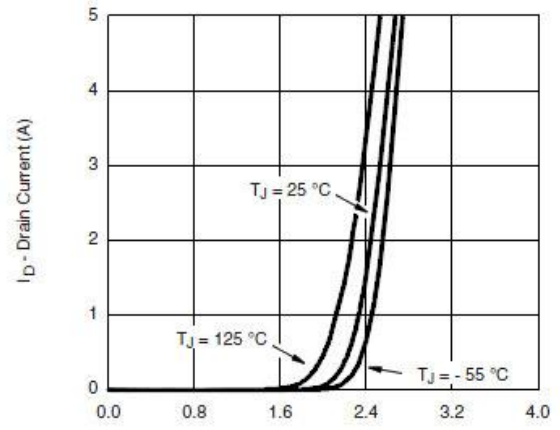
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D = -250\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D = -250\mu\text{A}$	-1.0		-3.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -32V, V_{GS} = 0V$			-1	uA
		$V_{DS} = -32V, V_{GS} = 0V, T_J = 85^{\circ}\text{C}$			-20	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq -5V, V_{GS} = -10V$	-20			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = 10A$		32	38	m $\Omega$
		$V_{GS} = -4.5V, I_D = -8A$		42	54	
Forward Transconductance	$g_{FS}$	$V_{DS} = -15V, I_D = -5A$		20		S
Diode Forward Voltage	$V_{SD}$	$I_S = -2A, V_{GS} = 0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = -20V, V_{GS} = -4.5V, I_D = -5.0A$		13	20	nC
Gate-Source Charge	$Q_{gs}$			4.5		
Gate-Drain Charge	$Q_{gd}$			6.5		
Input Capacitance	$C_{iss}$	$V_{DS} = -20V, V_{GS} = 0V, f = 1\text{MHz}$		1100		pF
Output Capacitance	$C_{oss}$			145		
Reverse Transfer Capacitance	$C_{rss}$			115		
Turn-On Time	$t_{d(on)}$	$V_{DD} = -20V, R_L = 4\Omega, I_D = -5.0A,$ $V_{GEN} = -4.5V, R_G = 1\Omega$		40	80	ns
	$t_r$			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	$t_f$		12	20		



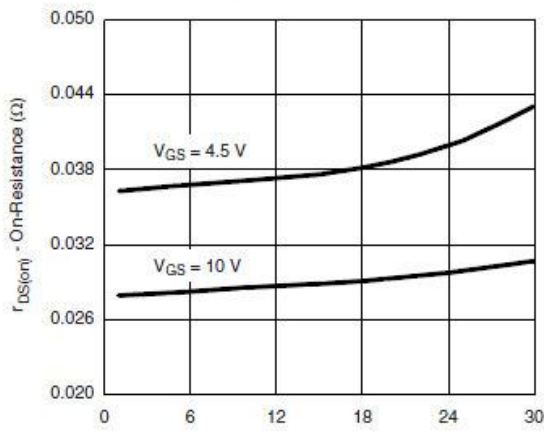
● Typical Characteristics



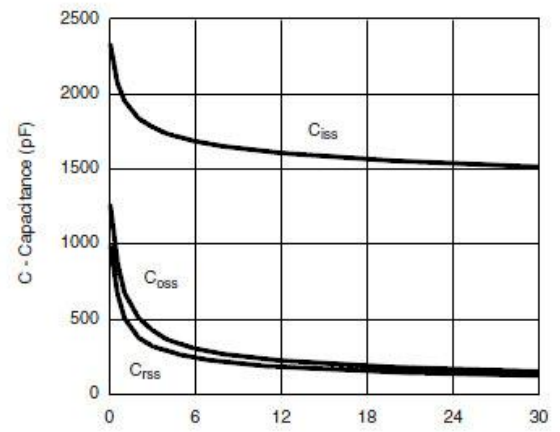
Output Characteristics



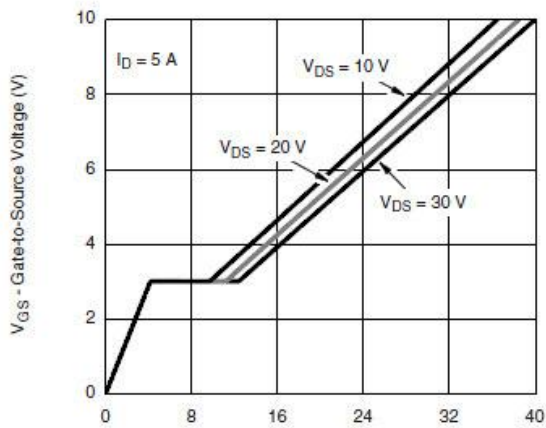
Transfer Characteristics



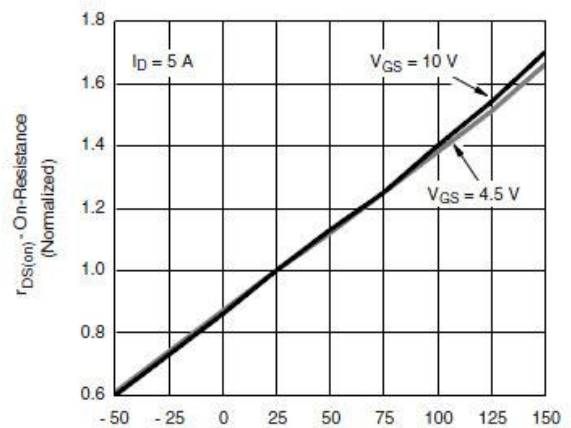
On-Resistance vs. Drain Current



Capacitance



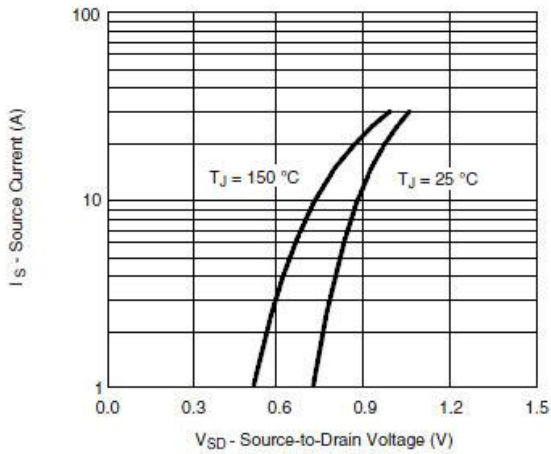
Gate Charge



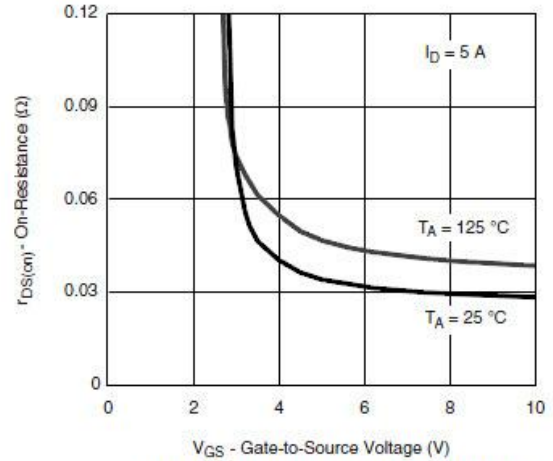
On-Resistance vs. Junction Temperature



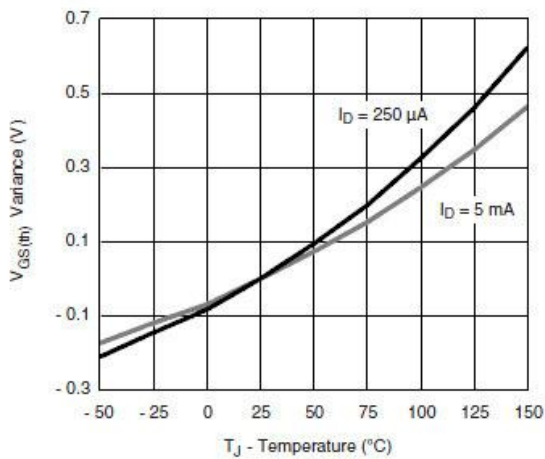
● Typical Characteristics



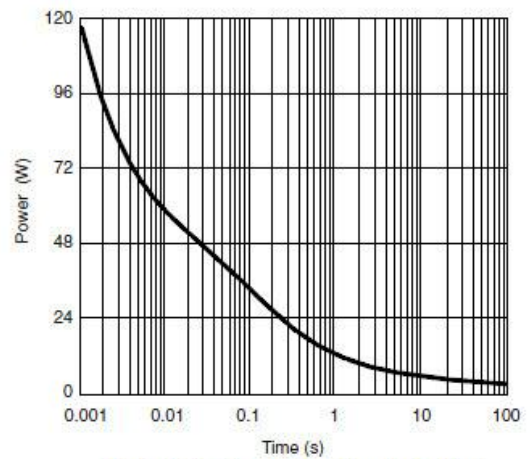
Source-Drain Diode Forward Voltage



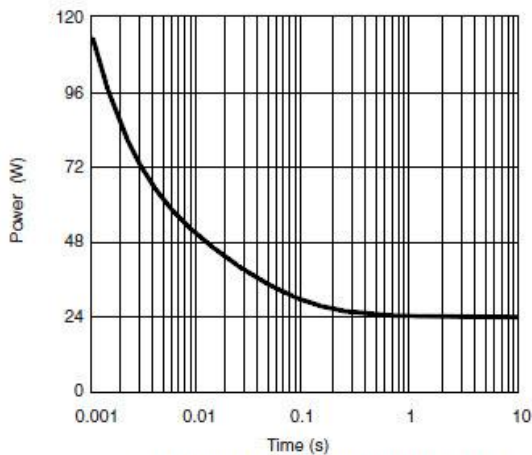
On-Resistance vs. Gate-to-Source Voltage



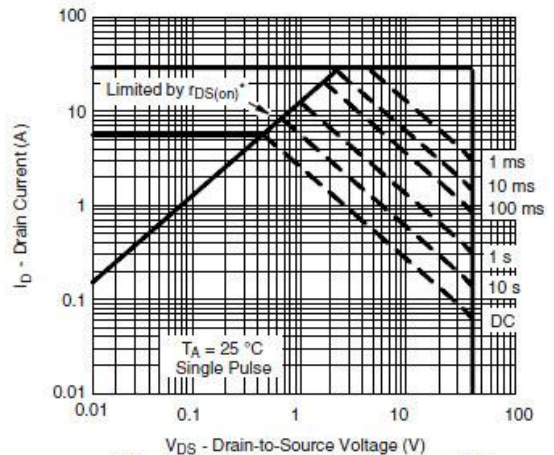
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



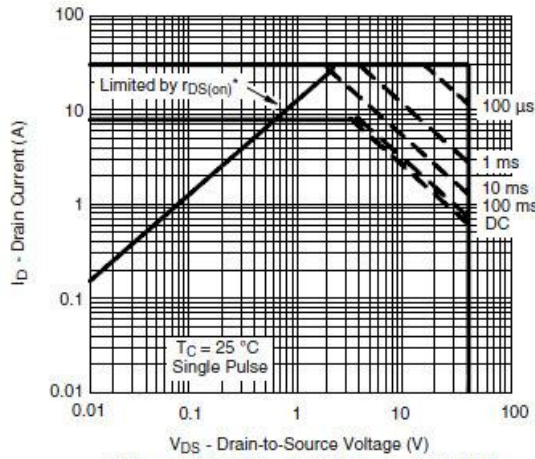
Single Pulse Power, Junction-to-Case



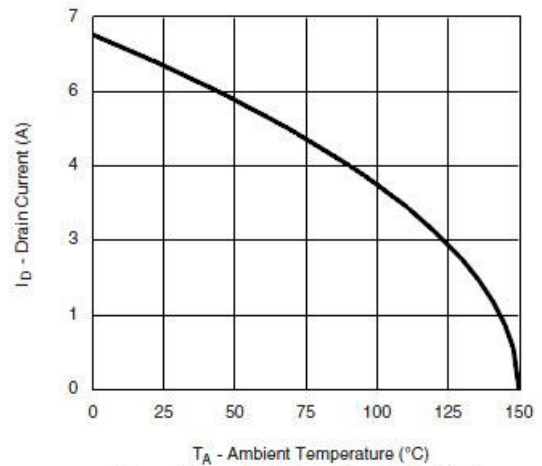
Safe Operating Area, Junction-to-Ambient



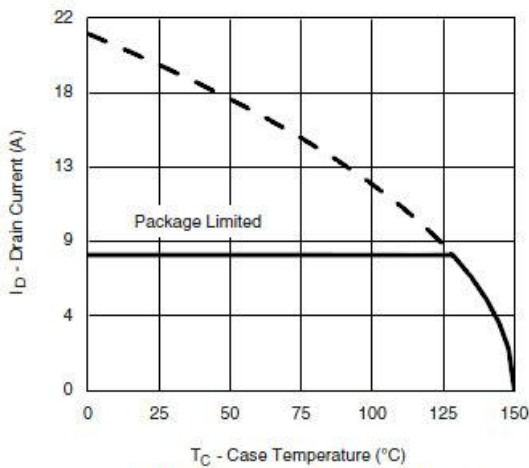
● Typical Characteristics



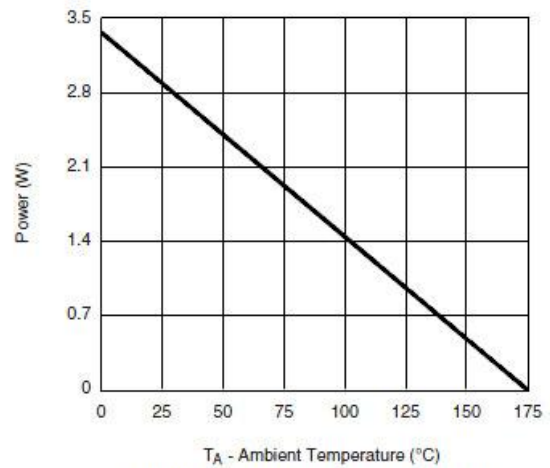
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Case**



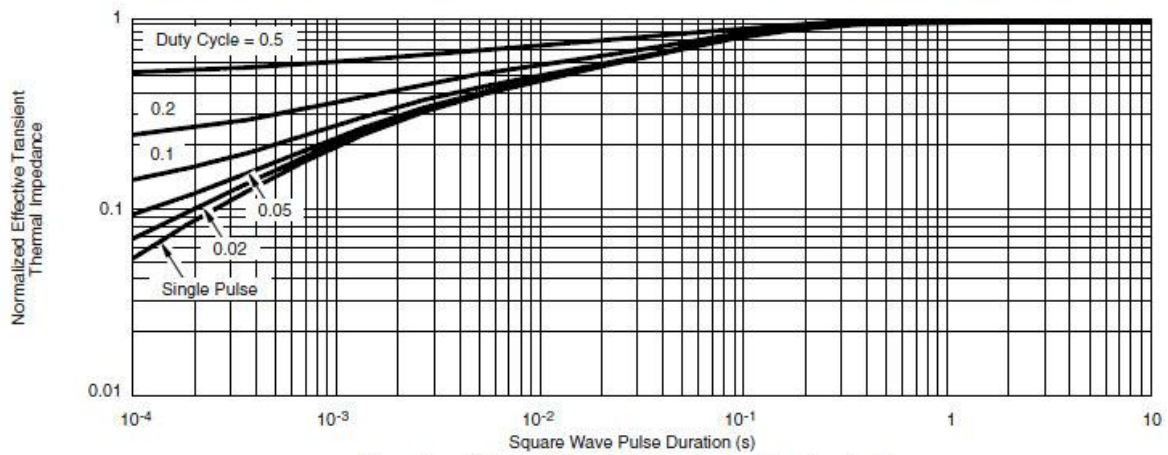
**Current Derating\*, Junction-to-Ambient**



**Current Derating\*, Junction-to-Case**



**Power Derating\*, Junction-to-Ambient**

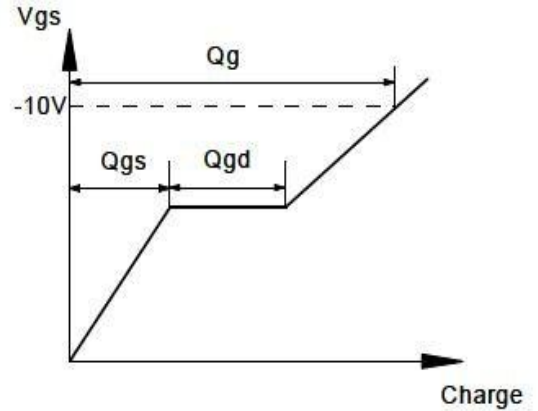
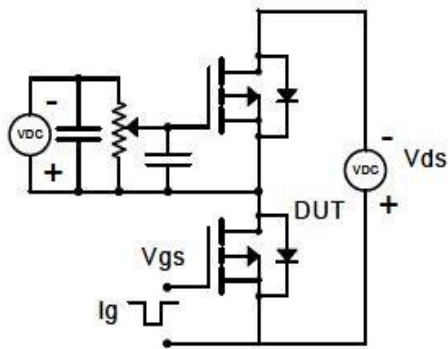


**Normalized Thermal Transient Impedance, Junction-to-Case**

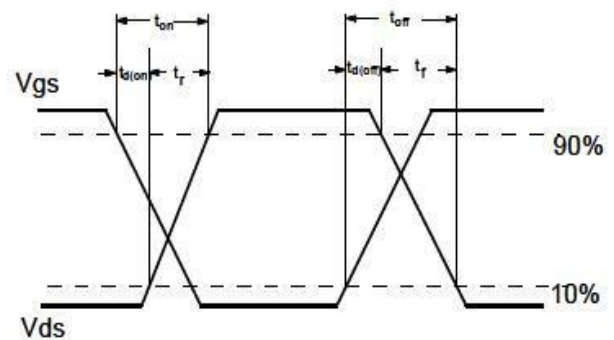
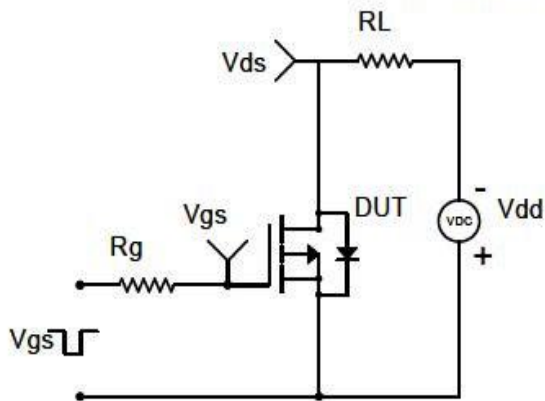


- Typical Characteristics

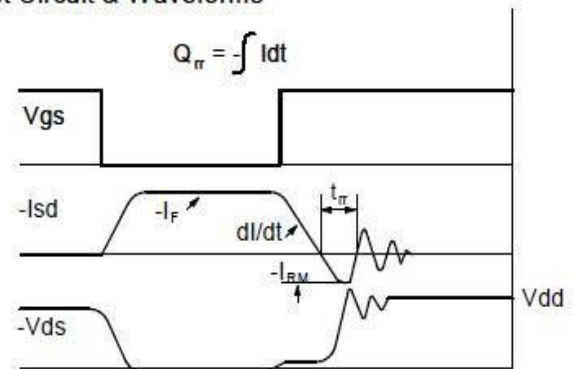
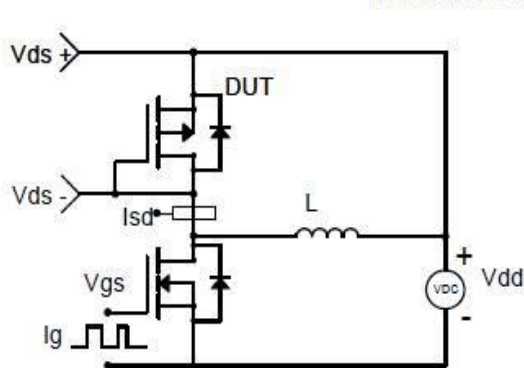
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

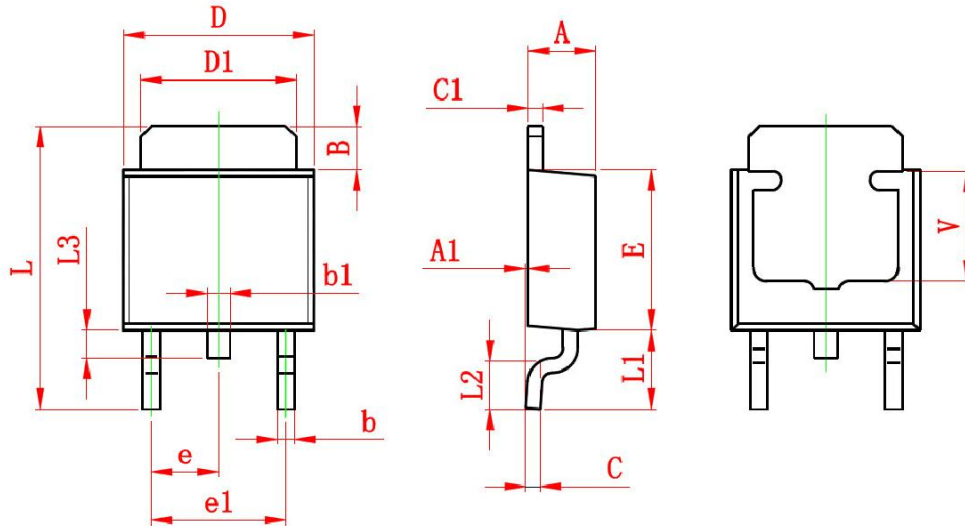


Diode Recovery Test Circuit & Waveforms





● Package Information ( TO-252-2L )



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	