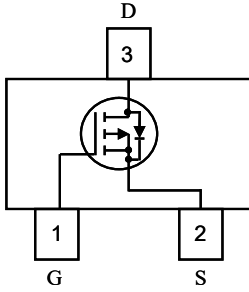


P-Channel Enhancement Mode Field Effect Transistor

<p>● Features</p> <p>$V_{DS} (V) = -30 V$ $I_D = -4.2 A$ $R_{DS(ON)} = 50m \Omega @V_{GS} = -10V$ $R_{DS(ON)} = 70m \Omega @V_{GS} = -4.5V$ High density cell design for low $R_{DS(ON)}$.</p>	<p>● General Description</p> <p>This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance.</p> <p>This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.</p>
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<p>● Pin Configurations</p> <div style="text-align: center;">  <p>SOT23</p> </div>
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● **Absolute Maximum Ratings @ $T_A=25^\circ C$ unless otherwise noted**

Parameter	Symbol	Ratings	Unit	
Drain-Source Voltage	V_{DSS}	-30	V	
Gate-Source Voltage	V_{GSS}	± 20	V	
Drain Current		Continuous	-4.2	A
		Pulsed ⁽¹⁾	-10	
Power Dissipation	P_D	350	mW	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$	

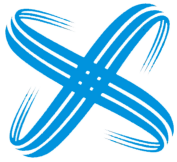


● **Electrical Characteristics** @ $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
Gate - Body Leakage, Forward	I_{GSSF}	$V_{GS} = +20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (2)						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.6	-2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.2\text{ A}$		70	95	m Ω
		$V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$		50	60	
Forward Transconductance	G_{FS}	$V_{DS} = -5\text{ V}, I_D = -2.8\text{ A}$	4	6		S
DYNAMIC CHARACTERISTICS (3)						
Input Capacitance	C_{ISS}	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, F = 1.0\text{ MHz}$		680		pF
Output Capacitance	C_{OSS}		--	72		pF
Reverse Transfer Capacitance	C_{RSS}			58		pF
SWITCHING CHARACTERISTICS (3)						
Turn-On Delay Time	$T_{D(ON)}$	$V_{DD} = -6\text{ V}, R_L = 6\ \Omega, I_D = -1.0\text{ A},$ $V_{GEN} = -4.5\text{ V}, R_G = 6\ \Omega$	--		20	ns
Turn-On Rise Time	T_R				10	
Turn-Off Delay Time	$T_{D(OFF)}$	$V_{DD} = -6\text{ V}, R_L = 6\ \Omega, I_D = -1.0\text{ A},$ $V_{GEN} = -4.5\text{ V}, R_G = 6\ \Omega$	--		65	ns
Turn-Off Fall Time	T_F				45	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Current(4)	I_S	--			-1.35	A
Drain-Source Diode Forward Voltage(2)	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -0.75\text{ A}$	-0.6	-0.8	-1.3	V

Notes

- 1、Pulse width limited by maximum junction temperature.
- 2、Pulse test: $PW \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- 3、Guaranteed by design, not subject to production testing.
- 4、Surface Mounted on FR4 Board, $T < 5\text{ sec}$.



● Typical Performance Characteristics (TJ =25 Noted)

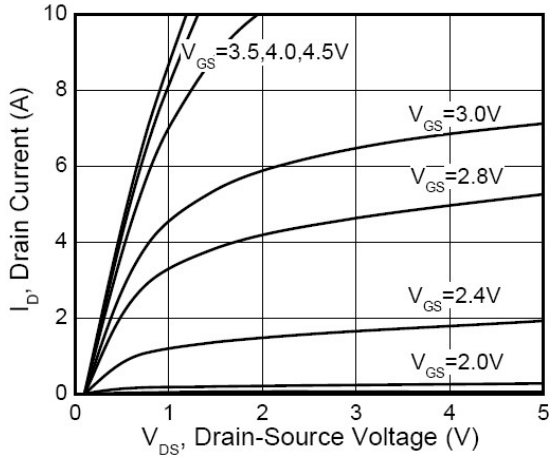


Figure 1. Output Characteristics

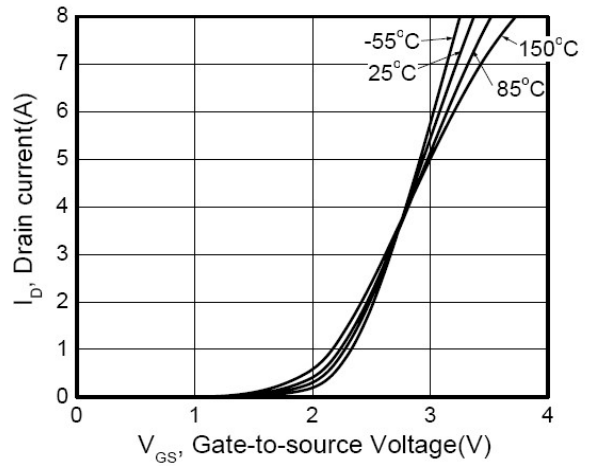


Figure 2. Transfer Characteristics

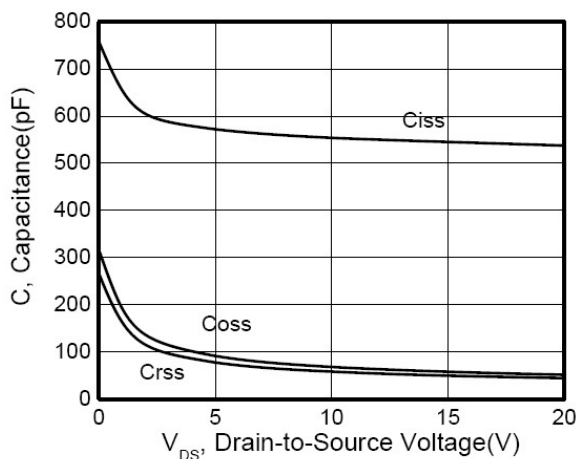


Figure 3. Capacitance

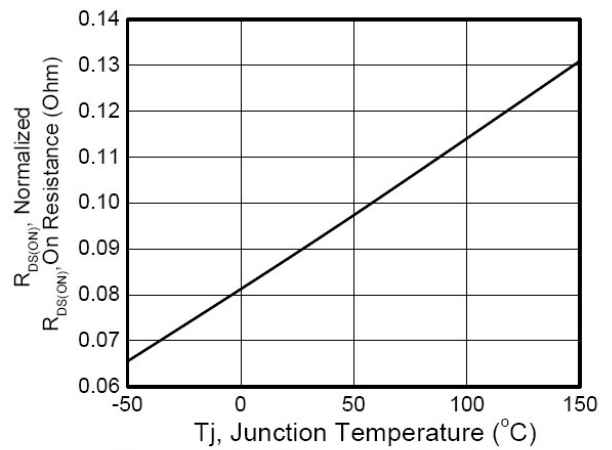


Figure 4. On Resistance Vs. Temperature

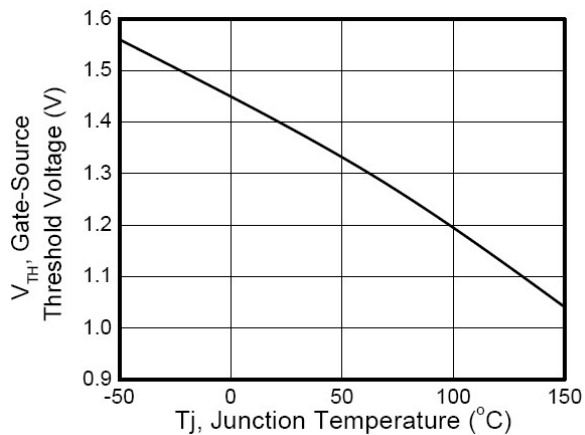


Figure 5. Gate Thershold Vs. Temperature

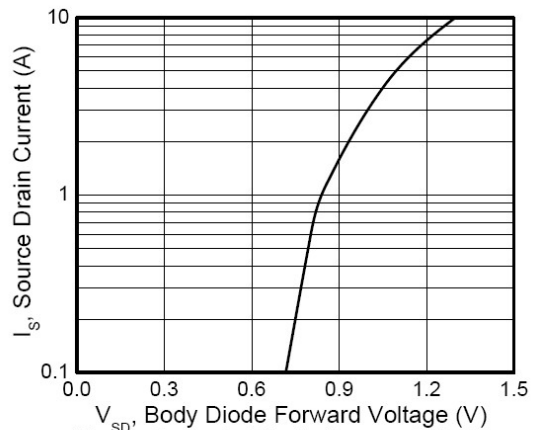


Figure 6. Body Diode Forward Voltage Vs. Source Current