P-Mos With Gate Protect Diode

Features

-20V/-4A,$R_{DS(ON)}$=35mΩ @V_{GS}=-4.5V
-20V/-4A,$R_{DS(ON)}$=45mΩ @V_{GS}=-2.5V
-20V/-2A,$R_{DS(ON)}$=54mΩ @V_{GS}=-1.8V
high density cell design for extremely low $R_{DS(ON)}$
Exceptional on-resistance and maximum DC current capability
ESD Rating：2000V HBM

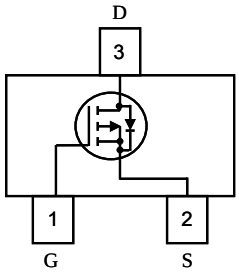
APPLICATIONS

Power Management in Note book
Portable Equipment
Battery Powered System
DC/DC Converter
Load Switch
DSC ,LCD Display inverter

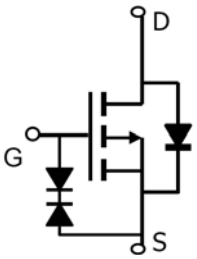
General Description

The FS2209 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

Pin Configurations



SOT23



ESD Rating：2000V HBM

Absolute Maximum Ratings @T_A=25℃ unless otherwise noted

Parameter	Symbol	Ratings	Unit
Drain - Source Voltage	V_{DSS}	-20	V
Gate –Source Voltage	V_{GS}	±8	V
Drain Current (Continuous)	I_D	-4	A
Drain Current (Pulse)	I_{DP}	-30	A
Power Dissipation	P_D	1.25	W
Operating Temperature	T_J	-55~150	℃
Storage Temperature	T_{STG}	-55~150	℃
ESD Rating：2000V HBM	-		

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.3	-0.55	-1	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-1	
		V_{DS}=-16V, V_{GS}=0V T_J=55℃			-10	
$I_{D(ON)}$	On-State Drain Current	V_{DS}=-5V, V_{GS}= -4.5V	-25			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D= -4.0A		35	43	mΩ
		V_{GS}=-2.5V, I_D= -4.0A		45	55	
		V_{GS}=-1.8V, I_D= -2.0A		54	75	
G_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4A	8	16		S
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.78	-1	V
DYNAMIC						
Q_g	Total Gate Charge	V_{DS}=-10V, V_{GS}=-4.5V, I_D=-4A		17.2		nC
Q_{gs}	Gate-Source Charge			1.3		
Q_{gd}	Gate-Drain Charge			4.5		
R_g	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		6.5		Ω
C_{iss}	Input Capacitance	V_{DS}=-10V, V_{GS}=0V, f=1MHz		1450		pF
C_{oss}	Output Capacitance			205		
C_{rss}	Reverse Transfer Capacitance			160		
$t_{d(on)}$	Turn-On Time	V_{DS}=-10V, R_L =2.5Ω R_{GEN}=3V, V_{GS}=-4.5V		9.5		ns
t_r				17		
$t_{d(off)}$	Turn-Off Time			94		
t_f				35		

Notes:

1. Pulse width limited by maximum junction temperature. Pulse test: PW≤300μs, duty cycle≤2%.
2. For design AID only, not subject to production testing. Switching time is essentially independent of operating temperature.

- **Typical Performance Characteristics**

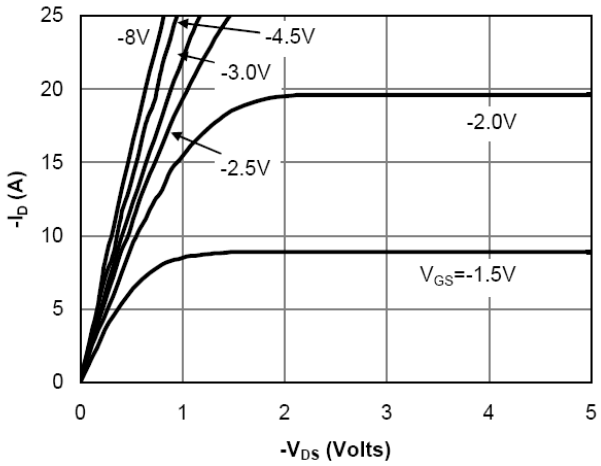


Fig 1: On-Region Characteristics

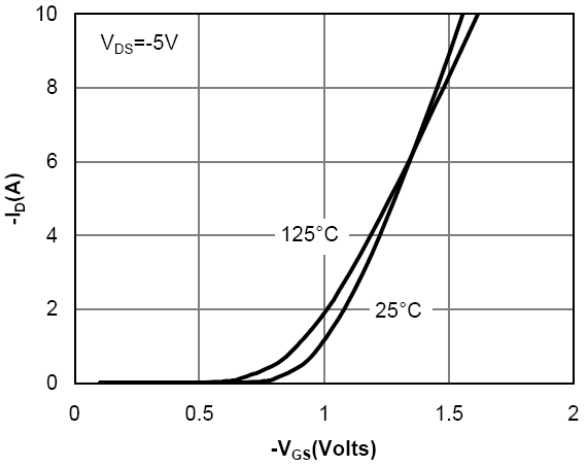


Figure 2: Transfer Characteristics

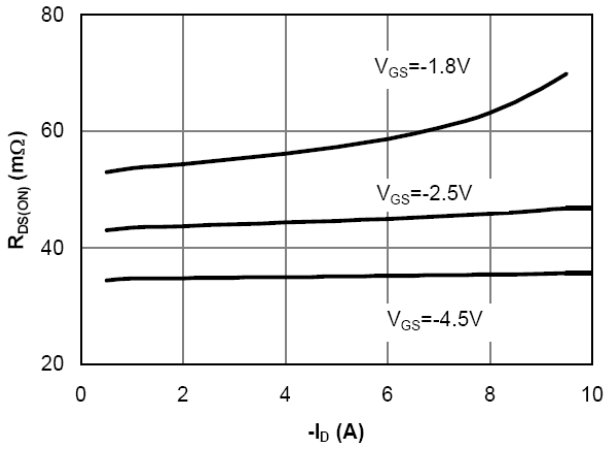


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

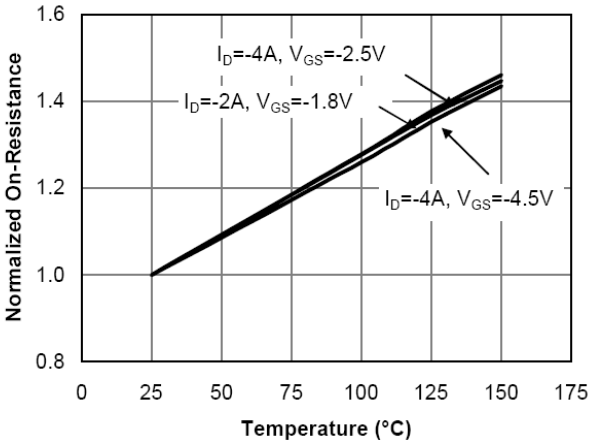


Figure 4: On-Resistance vs. Junction Temperature

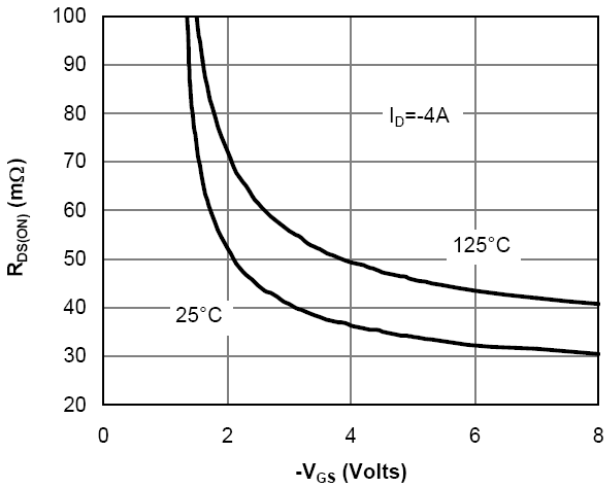


Figure 5: On-Resistance vs. Gate-Source Voltage

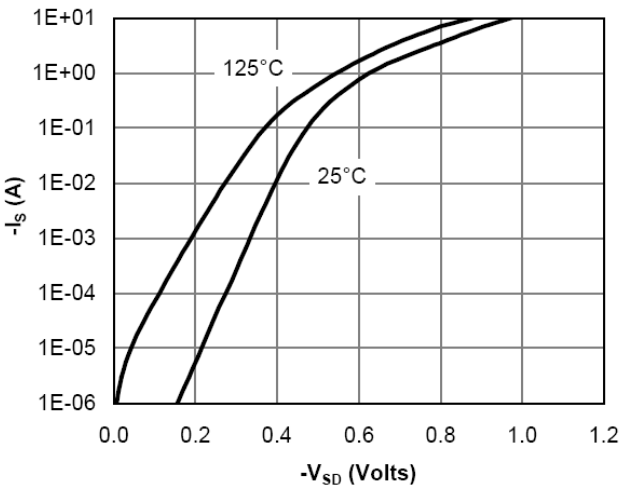
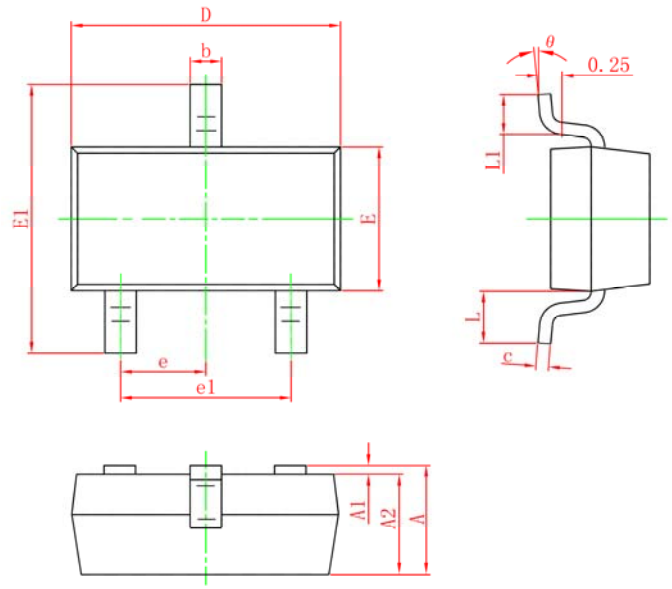


Figure 6: Body-Diode Characteristics

- **Package Information**

SOT-23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°
UNIT:mm				