Ultra-Small High-Precision Voltage Detector

Features

Ultra-low current consumption: 1.0μA@3.5V(typ)
High-precision detection voltage: ±2.0 %
Hysteresis characteristics: -VDET ×5%(typ)
Operating voltage range: 0.95 V to 8.0 V
Detection voltage: 1.5V to 6.0 V (0.1 V step)
Output forms:
NMOS open-drain output (Active Low)
CMOS output (Active Low)

Applications

Memory battery back-up circuits
Power-on reset circuits
Power failure detection
Power monitor for portable equipment such as notebook computers, digital cameras, PDA, and cellular phones.
Constant voltage power monitors for cameras, video equipment and communication devices.
Power monitor for microcomputers and reset for CPUs.

General Description

The FS8808 Series is a series of high-precision voltage detectors developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0 %. Two output forms, Nch open-drain and CMOS output, are available.

Ordering Information

FS8808①②③④⑤⑥⑦

DESIGNATOR	SYMBOL	DESCRIPTION
①	Pin Type:	A: Normal; B: B-Type
②③④	Output Detection Voltage	….200=2.0V, 250=2.5V, 263=2.63V 293=2.93V％0.1V step）…….
⑤	Type of output	N: Nch pen-drain, C: CMOS output
⑥⑦	Package Type:	ST:SOT343、SI: SOT23、SM:SOT89、TA:TO92

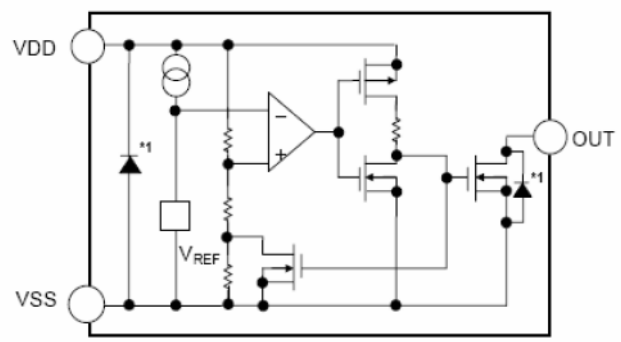
Absolute Maximum Ratings

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		VDD	VSS－0.3 ~ VSS＋10	V
Output voltage		VOUT	VSS－0.3 ~ VSS＋10	V
Power dissipation	SOT-23-3	PD	250	mW
	SOT-89		500	mW
	TO-92		500	mW
	SOT343		250	mW
Operating ambient temperature		Topr	－40 ~＋85	°C
Storage temperature		Tstg	－40 ~＋125	°C

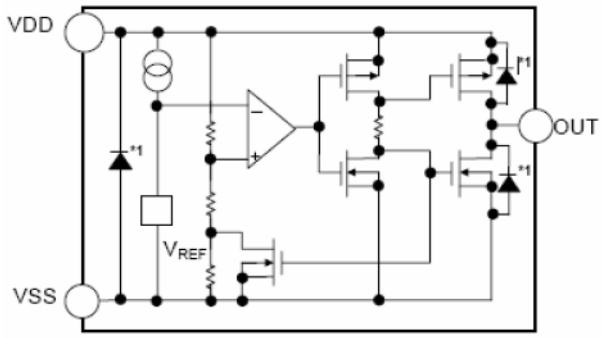
- **Electrical Characteristics** @ (TA=25°C, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Detection voltage*1	$-V_{DET}$	—		$-V_{DET(S)}\times0.98$	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.02	V
Hysteresis width	V_{HYS}	—		0.02× $-V_{DET(S)}$	0.05× $-V_{DET(S)}$	0.08× $-V_{DET(S)}$	V
Current consumption	I_{SS}	V_{DD} =－V_{DET}＋0.5V	FS8808C/N20～26	—	1.0	2.0	uA
			FS8808 C/N 26～39	—	1.2	2.5	uA
			FS8808 C/N 39～60	—	1.5	3.0	uA
Operating voltage	V_{DD}	—		0.95	—	8	V
Output current	I_{OUT}	NMOS：V_{OUT} =0.5 V V_{DD} =－V_{DET}－0.5 V	FS8808 C/N 20～26	3.0	13.0	—	mA
			FS8808 C/N 26～39	3.0	15.0	—	mA
			FS8808 C/N 39～60	3.0	18.0	—	mA
		PMOS：V_{DD}－V_{OUT} =0.5 V V_{DD} =－V_{DET}＋0.5 V	FS8808 C/N 20～26	1.5	4.0	—	mA
			FS8808 C/N 26～39	1.5	6.0	—	mA
			FS8808 C/N 39～60	1.5	8.0	—	mA
Leakage current	I_{LEAK}	Only for NMOS open-drain output products, V_{DD} =8.0 V, V_{OUT} =8.0 V			—	0.1	uA
temperature coefficient		Ta=−40°C ~ +85°C		—	±120	±360	ppm/ °C
Delay time	T_D					200	uS

- **Typical Block Diagram**



Nch open-drain

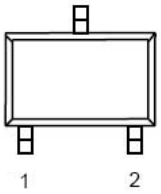


CMOS output

Note:*1-parasitic diode

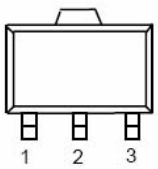
- **Pin Description**

SOT-23-3
Top view



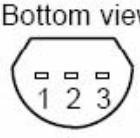
PIN NO.	A	B	Functions
1	VOUT	-	Voltage detection output pin
	-	VSS	GND pin
2	-	VOUT	Voltage detection output pin
	VSS	-	GND pin
3	VDD	VDD	Voltage input pin

SOT-89-3
Top view

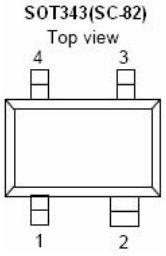


PIN NO	P	Functions
1	VOUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin

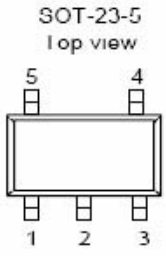
TO-92
Bottom view



PIN NO	T	TA	Functions
1	VOUT	-	Voltage detection output pin
	-	VDD	Voltage input pin
2	VDD	-	Voltage input pin
	-	VSS	GND pin
3	VSS	-	GND pin
	-	VOUT	Voltage detection output pin



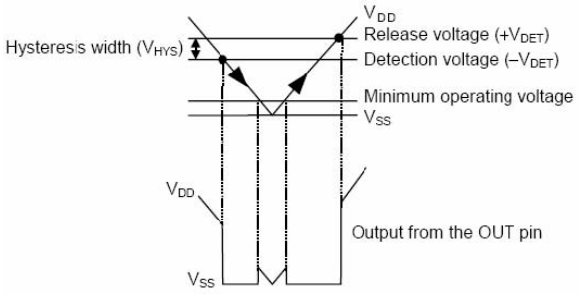
PIN NO	N	Functions
1	VOUT	Voltage detection output pin
2	VDD	Voltage input pin
3	NC	No Connection
4	VSS	GND pin



PIN NO.	MR	Functions
1	VOUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin
4	NC	No connection
5	NC	No connection

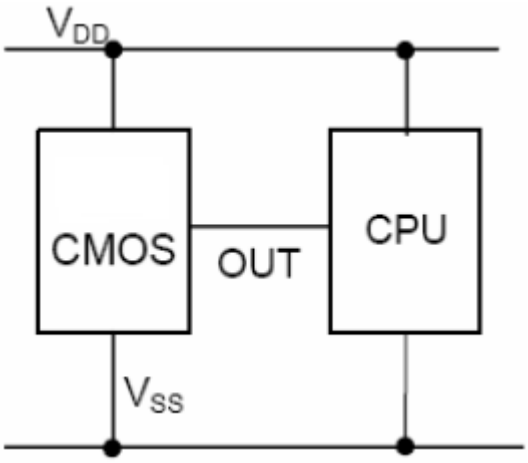
● Function Description

1. When a voltage higher than the release voltage (+VDET) is applied to the voltage input pin (VDD), the voltage will gradually fall..When a voltage higher than the detect voltage (-VDET) is applied to VDD , output (VOUT) will be equal to the input at VDD. Note that high impedance exists at VOUT with the N-channel open drain configuration. If the pin is pulled up, VOUT T will be equal to the pull up voltage.
2. When VDD falls below -VDET , VOUT will be equal to the ground voltage (VSS) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When VDD falls to a level below that of the minimum operating voltage (VMIN) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
4. When VDD rises above the VSS level (excepting levels lower than minimum operating voltage), VOUT will be equal to VSS until VDD reaches the +VDET level.
5 . Although VDD will rise to a level higher than +VDET, VOUT maintains ground voltage level via the delay circuit.
6. Following transient delay time, VDD will be output at VOUT. Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

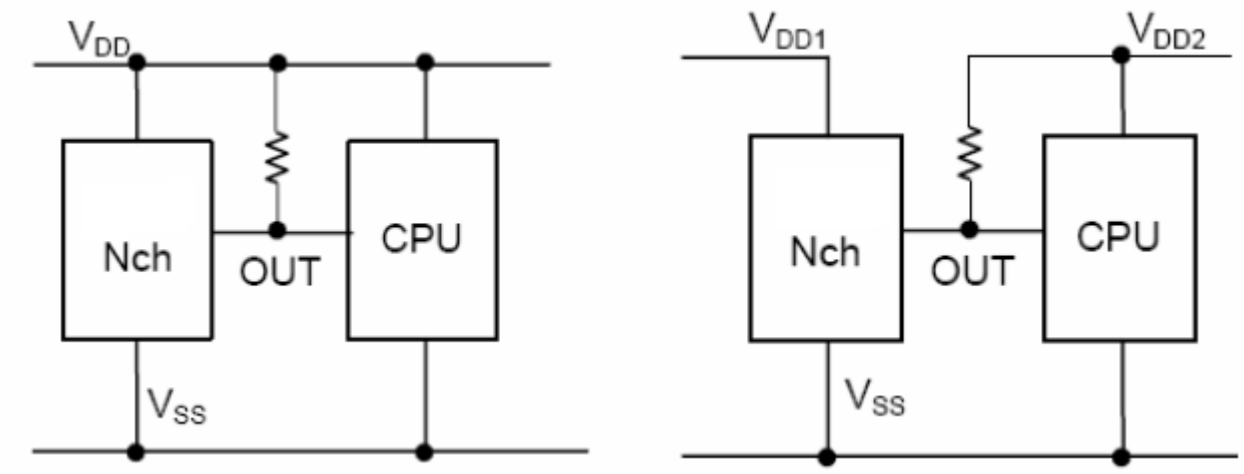


- **Typical Application Circuit**

1、 CMOS output：

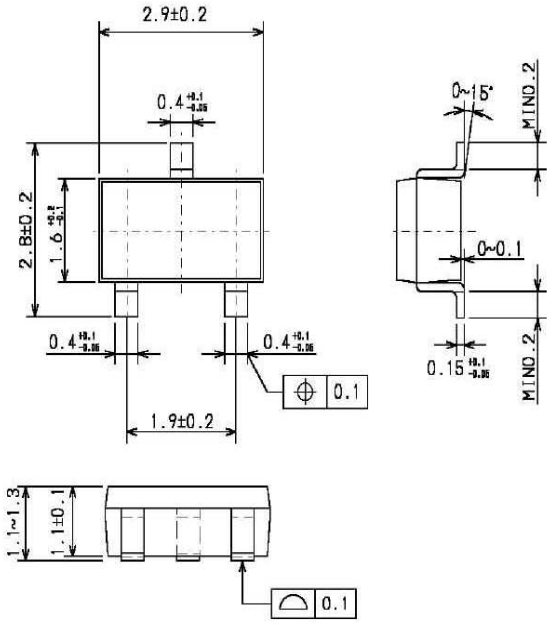


2、 Nch open-drain

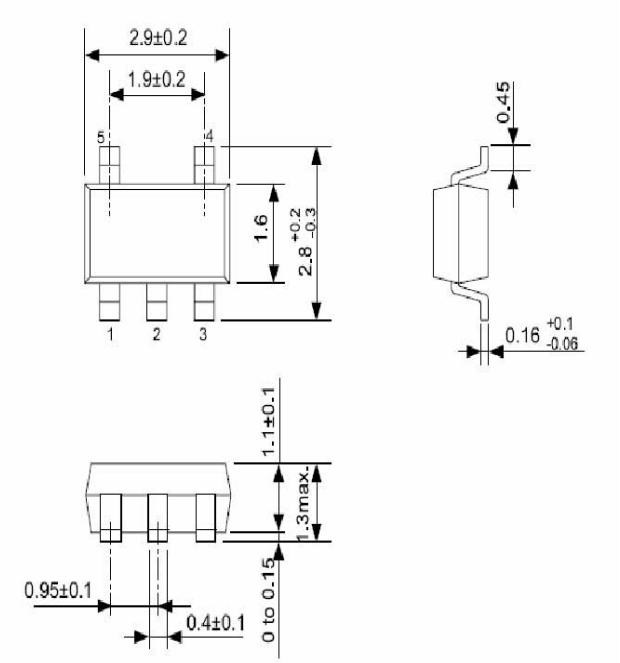


- **Package Information**

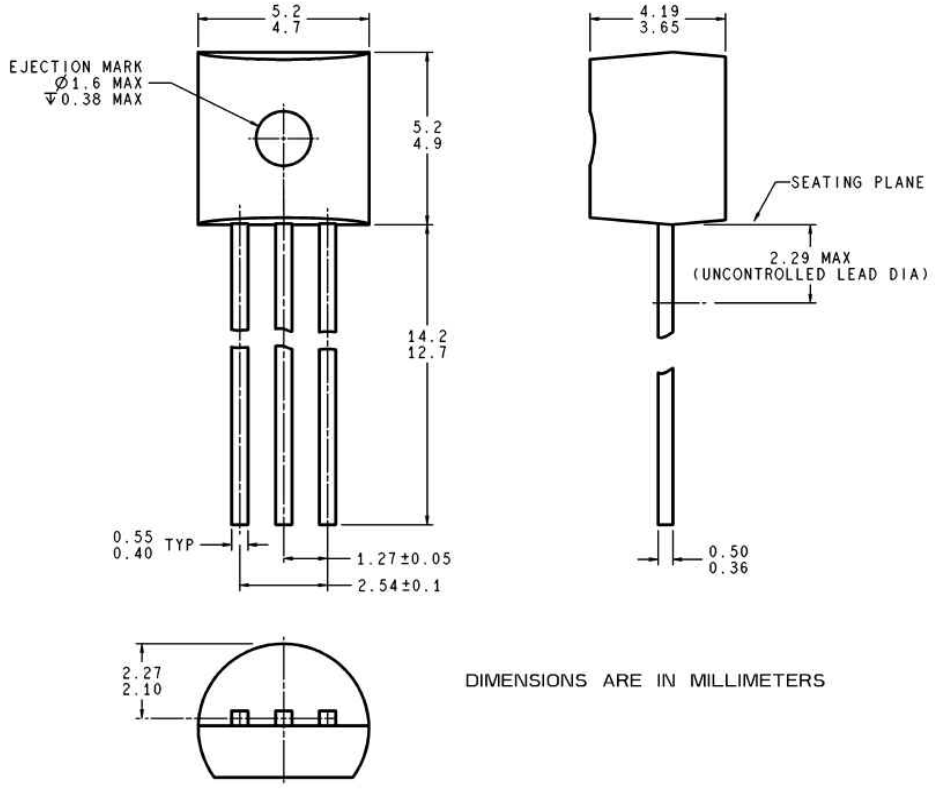
• SOT-23



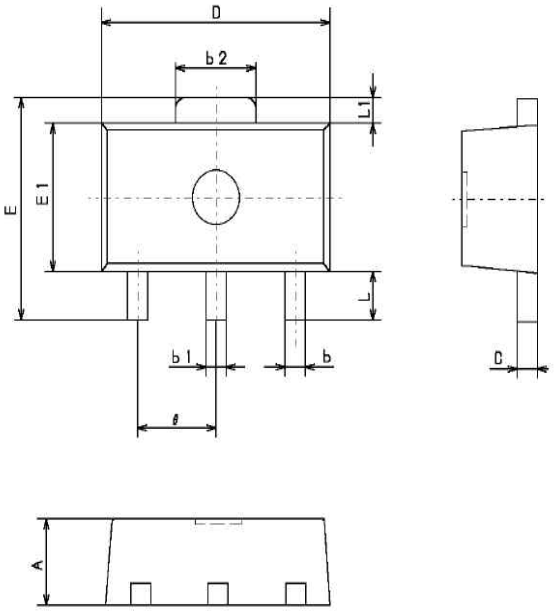
SOT23-5



• TO-92



● SOT-89



Symbols	Dimensions in millimeters		
	Min	Nom	Max
A	1.40	1.50	1.60
b	0.36	0.42	0.48
b1	0.41	0.47	0.53
b2	1.40	1.60	1.75
C	0.38	0.40	0.43
D	4.40	4.50	4.60
E	—	—	4.25
E1	2.40	2.50	2.60
θ	1.40	1.50	1.60
L	1.80	—	—
L1	—	0.40	—

● SOT343（SC-82）