Ultra-Small Built-In Delay High-Precision Voltage Detector

Features

Ultra-low current consumption: 1.0μA@3.5V(typ)
High-precision detection voltage: ±2.0 %
Hysteresis characteristics: -V_{DET} ×5%(typ)
Operating voltage range: 0.95 V to 8.0 V
Detection voltage: 1.5V to 6.0 V (0.1 V step)
Delay time: 200 mS(typ)
Output forms:
NMOS open-drain output (Active Low)
CMOS output (Active Low)

Applications

Memory battery back-up circuits
Power-on reset circuits
Power failure detection
Power monitor for portable equipment such as notebook computers, digital cameras, PDA, and cellular phones.
Constant voltage power monitors for cameras, video equipment and communication devices.
Power monitor for microcomputers and reset for CPUs.

General Description

The FS8809 Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time. developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0 %. Internal oscillator and counter timer can delay the release signal without external parts, delay times 200 mS Two output forms, Nch pen-drain and CMOS output are available.

Ordering Information

FS8809①②③④⑤⑥⑦

DESIGNATOR	SYMBOL	DESCRIPTION
①	Pin Type:	A: Normal; B: B-Type
②③④	Output Detection Voltage	….200=2.0V, 250=2.5V, 263=2.63V 293=2.93V％0.1V step）…….
⑤	Type of output	N: Nch pen-drain, C: CMOS output
⑥⑦	Package Type:	SI: SOT23

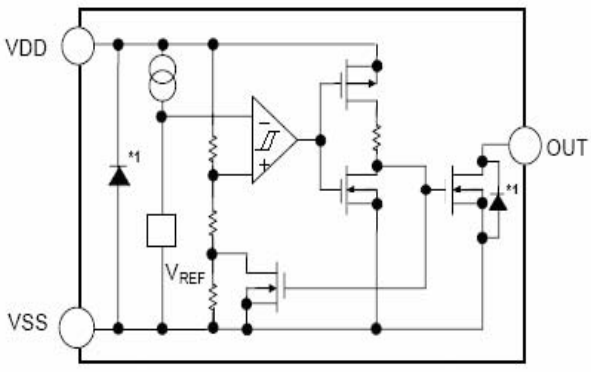
Absolute Maximum Ratings

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		V_{DD}	V_{SS}－0.3 ~ V_{SS}＋10	V
Output voltage		V_{OUT}	V_{SS}－0.3 ~ V_{SS}＋10	V
Power dissipation	SOT-23	P_D	250	mW
Operating ambient temperature		Topr	－40 ~＋85	°C
Storage temperature		Tstg	－40 ~＋125	°C

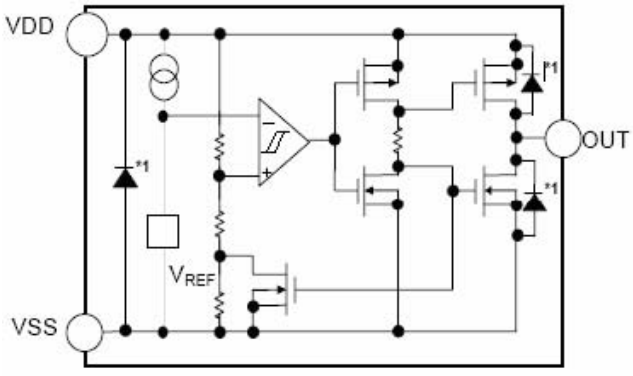
- **Electrical Characteristics** @ (T_A=25°C, unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Detection voltage*1	$-V_{DET}$	—		$-V_{DET(S)}$ ×0.98	$-V_{DET(S)}$	$-V_{DET(S)}$ ×1.02	V
Hysteresis width	V_{HYS}	—		0.02× $-V_{DET(S)}$	0.05× $-V_{DET(S)}$	0.08× $-V_{DET(S)}$	V
Current consumption	I_{SS}	V_{DD} =$-V_{DET}$+0.5V	FS8809 C/N20～26	—	1.0	2.0	uA
			FS8809 C/N 26～39	—	1.2	2.5	uA
			FS8809 C/N 39～60	—	1.5	3.0	uA
Operating voltage	V_{DD}	—		0.95	—	8	V
Output current	I_{OUT}	NMOS: V_{OUT} =0.5 V V_{DD} =$-V_{DET}$−0.5 V	FS8809 C/N 20～26	3.0	13.0	—	mA
			FS8809 C/N 26～39	3.0	15.0	—	mA
			FS8809 C/N 39～60	3.0	18.0	—	mA
		PMOS: V_{DD}−V_{OUT} =0.5 V V_{DD} =$-V_{DET}$+0.5 V	FS8809 C/N 20～26	1.5	4.0	—	mA
			FS8809 C/N 26～39	1.5	6.0	—	mA
			FS8809 C/N 39～60	1.5	8.0	—	mA
Leakage current	I_{LEAK}	Only for NMOS open-drain output products, V_{DD} =8.0 V, V_{OUT} =8.0 V			—	0.1	uA
temperature coefficient		Ta=−40°C ~ +85°C		—	±120	±360	ppm/ °C
Delay time	T_D				200		mS

- **Typical Block Diagram**

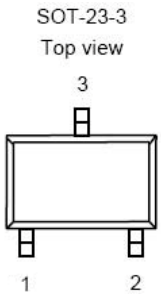


Nch open-drain



CMOS output

Pin Description



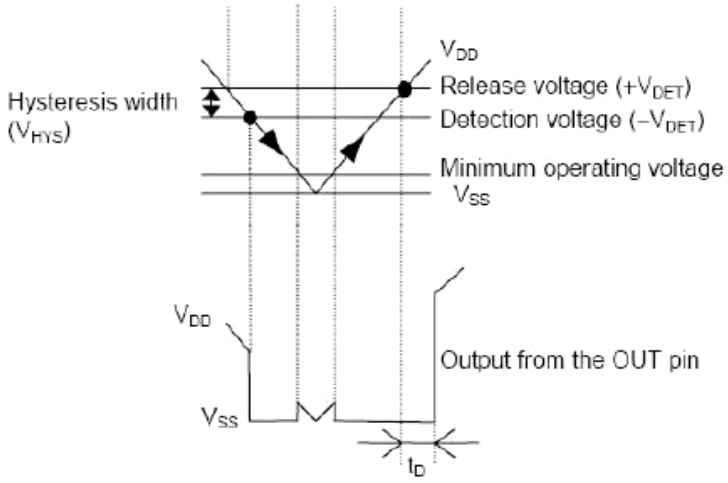
PIN NO.	A	B	Functions
1	VOUT	-	Voltage detection output pin
	-	VSS	GND pin
2	-	VOUT	Voltage detection output pin
	VSS	-	GND pin
3	VDD	VDD	Voltage input pin

Function Description

1. When a voltage higher than the release voltage ($+V_{DET}$) is applied to the voltage input pin (V_{DD}), the voltage will gradually fall..When a voltage higher than the detect voltage ($-V_{DET}$) is applied to V_{DD} , output (V_{OUT}) will be equal to the input at V_{DD}.
   Note that high impedance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.
2. When V_{DD} falls below $-V_{DET}$, V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When V_{DD} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
4. When V_{DD} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{DD} reaches the $+V_{DET}$ level.
5 . Although V_{DD} will rise to a level higher than $+V_{DET}$, V_{OUT} maintains ground voltage level via the delay circuit.
6. Following transient delay time, V_{DD} will be output at V_{OUT}.
   Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

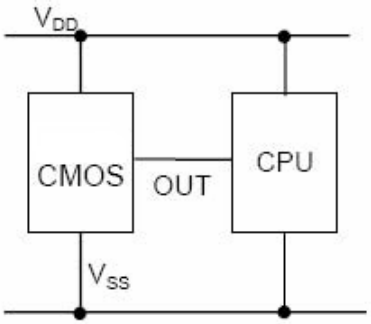
Notes :

1. The difference between $-V_{DET}$ and $+V_{DET}$ represents the hysteresis range.
2. Propagation delay time (t_D) represents the time it takes for V_{DD} to appear at V_{OUT} once the said voltage has exceeded the $+V_{DET}$ level.

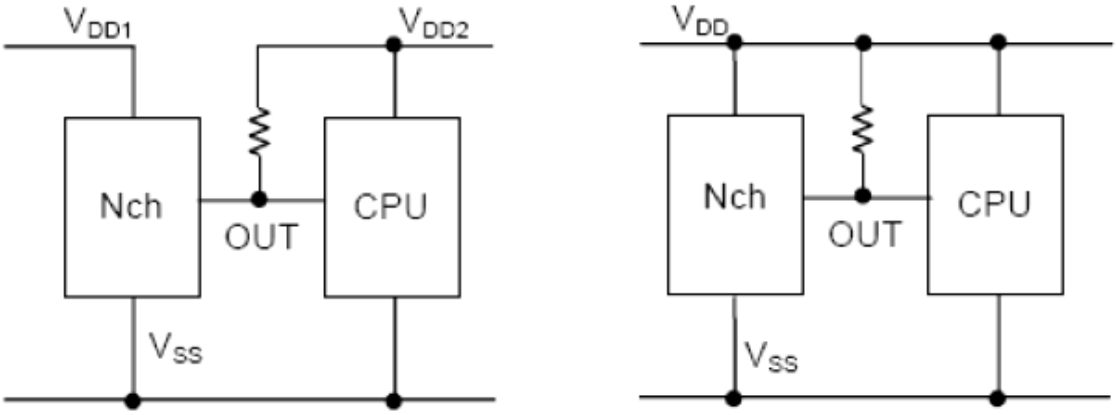


● Typical Application Circuit

1、 CMOS output：



2、 Nch open-drain



● Package Information

● SOT-23-3