Very High PSRR Ultra-Low Noise 500mA LDO

Features

- Up to 500mA Load Current
- Very Low IQ: 35μA
- Ultra Low Dropout: 330mV at 500mA Load
- Very High PSRR: 80db at 100Hz
- Ultra Low Noise: 45uVrms at 1.2V output
- Ultra-Fast Start-Up Time: 30μs
- Short Circuit and Overcurrent Protection
- Thermal Shutdown Protection
- 5kV HBM ESD Protection
- Ambient Temperature Range: -40°c To 85°C
- TSOT23-5, SOIC-8, and DFN package

Applications

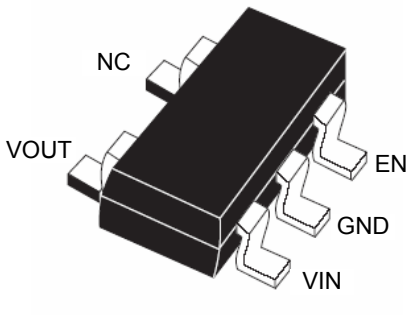
- LCD TV and monitors
- Handsets and IP Phones
- PCs and eBooks
- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable instruments

General Description

The FS3500xx family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection ratio (PSRR) while maintaining very low 35μA ground current. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The FS3500xx is stable with a 1.0μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to +125°C and is offered in a small SOT23-5, SOIC-8, and a ultra-small 2mm × 2mm DFN package with a thermal pad, which are ideal for small form factor portable equipment such as wireless handsets and PDAs.

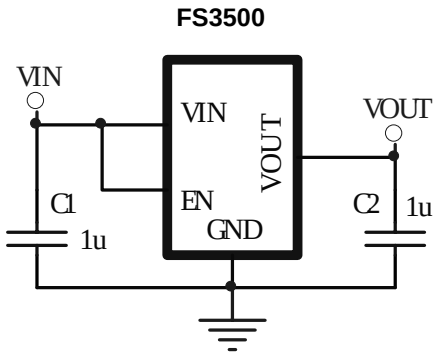
The FS3500xx is available in standard fixed output voltages of 1.2V, 1.5V, 1.8V, 2.5V), 2.8), 3.0V, 3.3V, and custom voltage options (50mV step options between 0.8V and 5.0V are available upon request).

Pin Configurations



SOT23-5L

Typical Application Circuit



Absolute Maximum Ratings

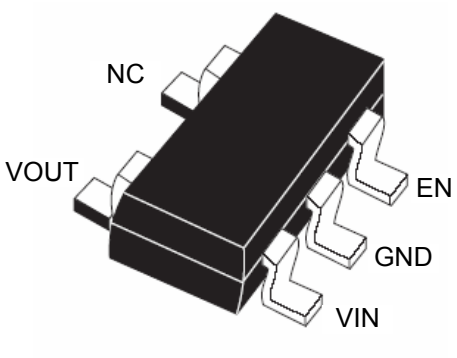
Parameter		Rating	Unit
IN Voltage		-0.3 to 6.5	V
Other Pin Voltage		-0.3 to V_{IN}+0.3	V
Maximum Load Current		800	mA
Junction to Ambient Thermal Resistance (θ_{JA}), TSOT23-5		230	°C/W
Junction to Ambient Thermal Resistance (θ_{JA}), SOIC-8		120	°C/W
Junction to Ambient Thermal Resistance (θ_{JA}), DFN2x2-6		130	°C/W
Operating Junction Temperature		-40 to 125	°C
Storage Temperature		-65 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
MSL Level (Note 2)		Refer to shipping label	
ESD Susceptibility	HBM (Human Body Model)	5	kV
	MM (Machine Model)	400	V

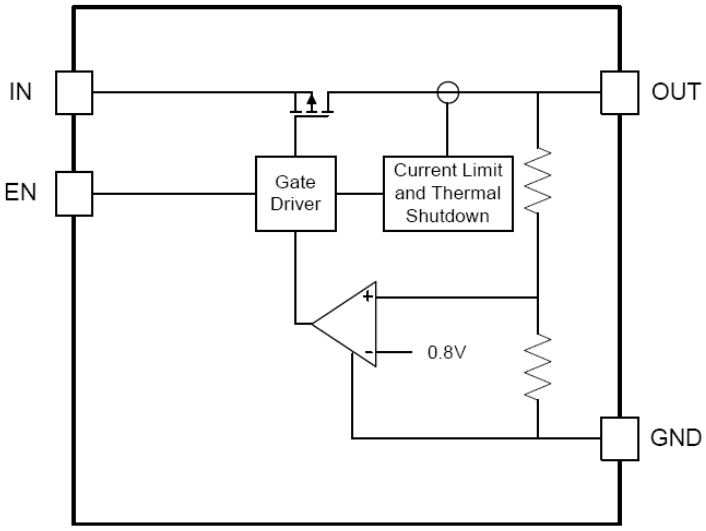
Electrical Characteristics

(V_{IN}= V_{EN} =3.6V, T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		2.5		6.0	V
Dropout Voltage	V_{DROP}	V_{OUT} ≥ 2.8V, I_{OUT} = 500mA		330	500	mV
		V_{OUT} ≥ 2.8V, I_{OUT} = 300mA		190	280	mV
DC Supply Quiescent Current	I_{Q_ON}	Active mode: V_{EN}=V_{IN}		35	49	μA
DC Supply Shutdown Current	I_{QOFF}	V_{EN}=0V		0.01	1	μA
Regulated Output Voltage	V_{OUT}	I_{OUT}=1mA, -40℃ □T_A□85℃	-2		2	%
Line Regulation		V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 10mA			0.4	%
Load Regulation		I_{OUT} from 0mA to 500mA			0.6	%
Soft-start Time		From Enable to Power On		30		μs
Current Limit		R_{LOAD}=1Ω	600	1000		mA
Power Supply Rejection Ratio	PSRR	f=100Hz, C_{OUT}=1μF, I_{OUT}=20mA		80		dB
		f=1kHz, C_{OUT}=1μF, I_{OUT}=20mA		70		dB
		f=10kHz, C_{OUT}=1μF, I_{OUT}=20mA		52		dB
		(10Hz to 100kHz C_{OUT} = 1μF)				
Output Noise		I_{OUT} = 200mA, V_{OUT}=2.8V,		70		μVRMS
		I_{OUT} = 200mA,V_{OUT}=1.2V		45		μVRMS
EN Low Threshold					0.4	V
EN High Threshold			1.4			V
EN Pin Input Current	I_{EN}			0	0.1	μA
Over-temperature Threshold	Shutdown			155		° C
Over-temperature Hysteresis				20		° C

- **Typical Block Diagram**

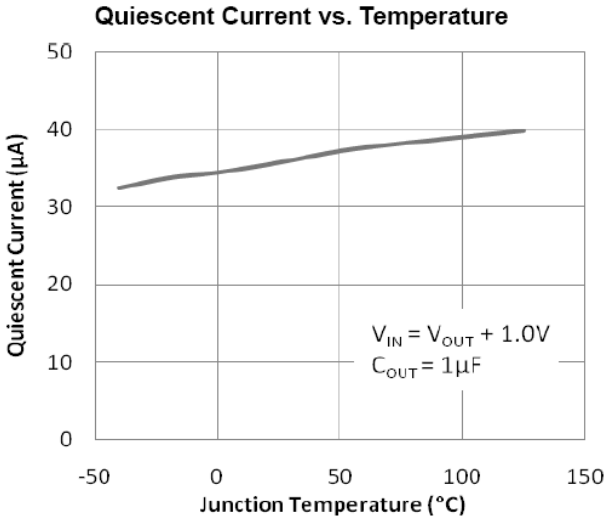


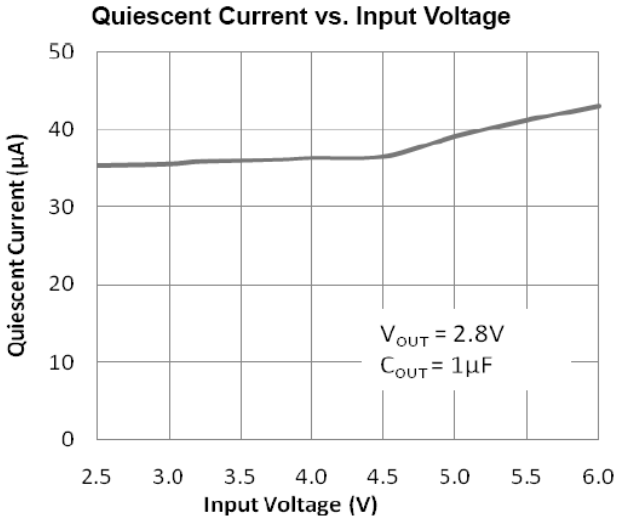


- **Pin Description**

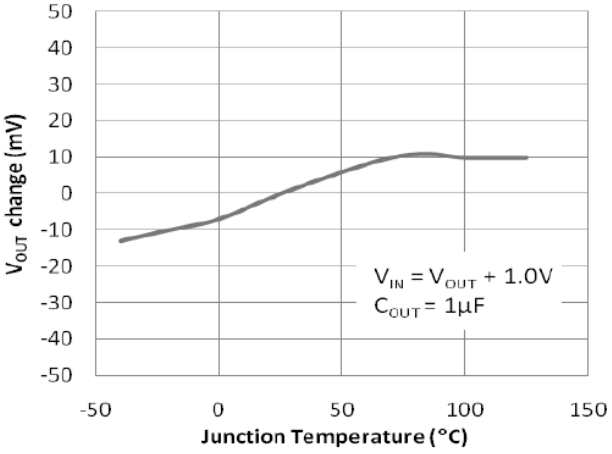
Pin No.		Name	Pin Function
TSOT23-5	DFN2x2-6		
1	3	IN	Input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor.
2	2	GND	Ground
3	1	EN	Enable control input, active high. Do not leave EN floating.
4	5, 6	NC	No connection
5	4	OUT	Output pin. Bypass a 1μF ceramic capacitor from this pin to ground.

- **Typical Performance Characteristics**

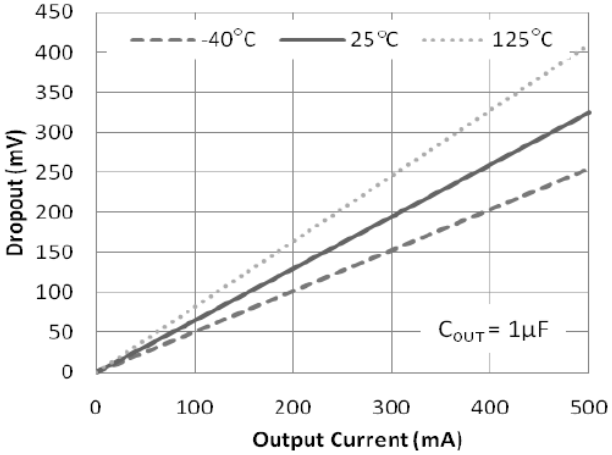




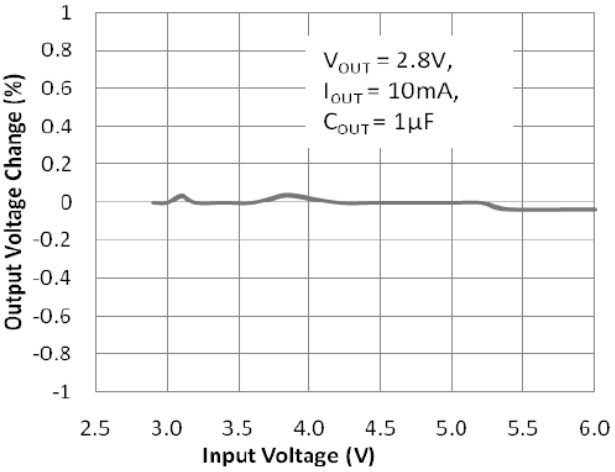
Output Voltage Change vs. Temperature



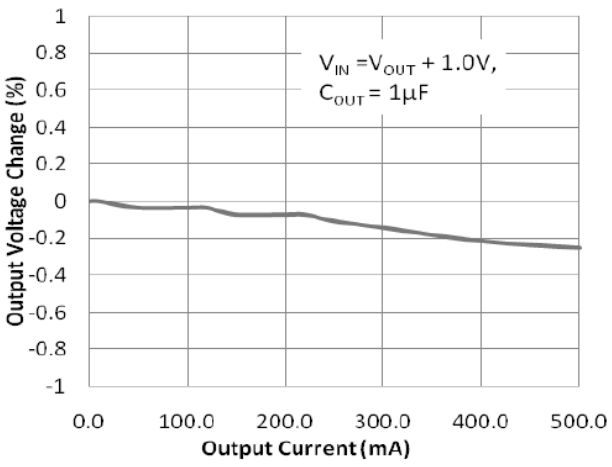
Dropout Voltage



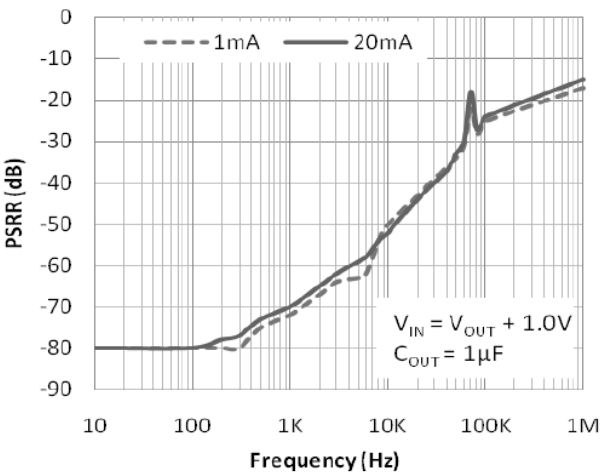
Line Regulation



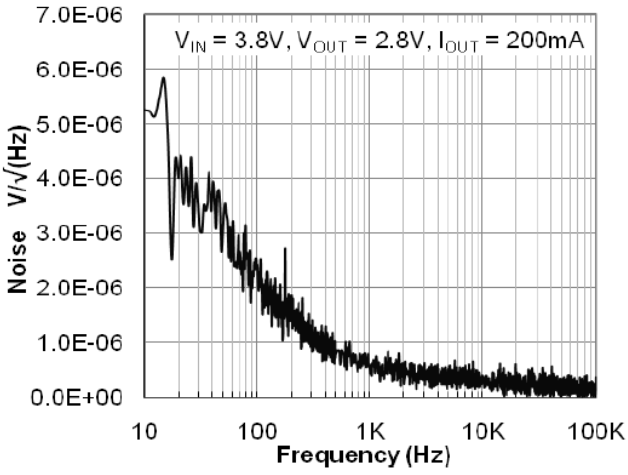
Load Regulation



Power Supply Ripple Rejection vs. Frequency



Output Noise Voltage



APPLICATION INFORMATION

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 2.2μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics is X7R or X5R. Higher capacitance values help to improve load/line transient response. Place output capacitor as close as possible to OUT and GND pins.

ON/OFF Input Operation

The FS3500XX is turned on by pulling up the EN pin to logic high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

High PSRR and Low Noise

RF circuits such as LNA (low-noise amplifier), up/down-converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires very high PSRR at RF power amplifier burst frequency. For instance, minimum 65dB PSRR at 217Hz is recommended for the GSM handsets. In order to provide good audio quality, the audio power supply for hand-free, game, MP3, and multimedia applications in cellular phones, require low-noise and high PSRR at audio frequency range (20Hz-20kHz). The FS3500XX, with PSRR of 80dB at 100Hz, is suitable for most of these applications that require high PSRR and low noise.

Ultra Fast Start-up

After enabled, the FS3500XX is able to provide full power in as little as tens of microseconds, typically 30μs. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100μA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs. The FS3500XX's fast transient response from 0 to 500mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate all the time. That requires LDO stays on at all times. However, in the standby mode, the microprocessor consumes only around 100~300μA. Since the phone stays in standby for the longest percentage of time, using a 40μA quiescent current LDO, instead of 100μA, saves 60μA and can substantially extends the battery standby time. The FS3500XX, consuming only around 35μA for all input range and output loading, provides great power saving in portable and low power applications.

Current Limit Protection

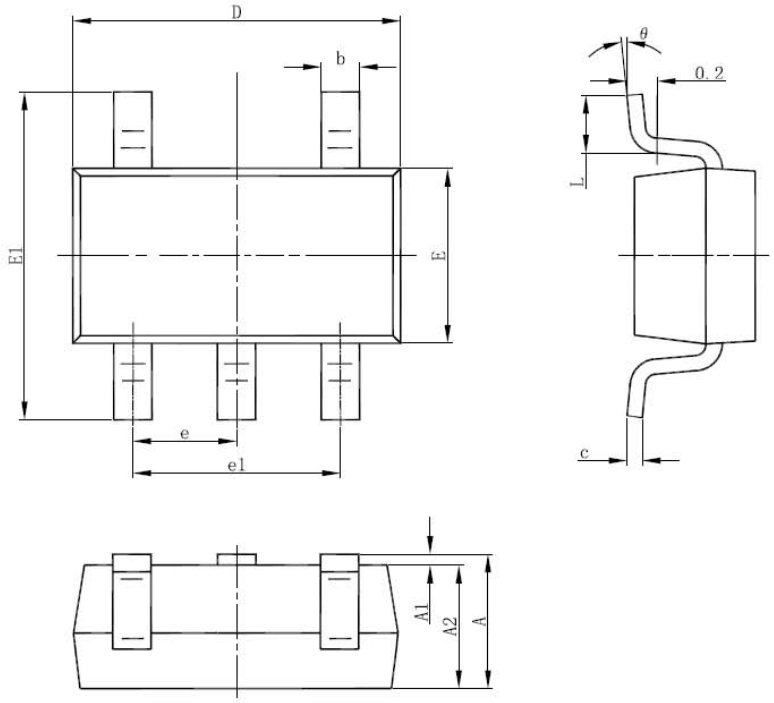
When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 500mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +135°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

- **Package Information**

SOT-23-5L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°