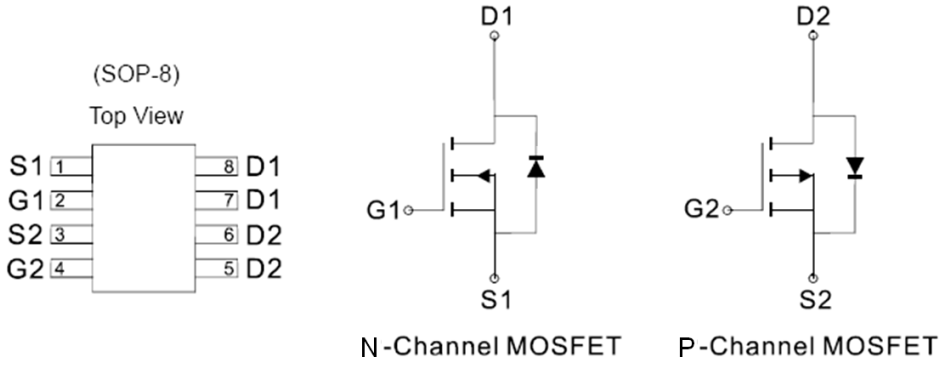
FORSEMI FS5505

40V N & P Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY			
FS5505	V(BR)DSS	RDS(ON)	ID
N-Channel	40	16mΩ	7.2A
P-Channel	-40	30mΩ	-6.5A

The FS5505 combines advanced trench MOSFET technology with a low resistance package to provide extremely low RDS(ON). this device is well suited for high current load applications.

- **Pin Configurations**



- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

PARAMETERS/TEST CONDITIONS		SYMBOL	N-Channel	P-Channel	UNITS
Drain-Source Voltage		VDS	40	-40	V
Gate-Source Voltage		VGS	±20	±20	V
Single Pulse Avalanche Energy		EAS	28	66	mJ
Avalanche Current		IAS	17.8	-27.2	A
Continuous Drain Current	TC = 25 °C	ID	7.2	-6.5	A
	TC =100 °C		5.6	-5.1	
Pulsed Drain Current1		IDM	14.5	-13	
Power Dissipation	TC = 25 °C	PD	2		W
	TC = 70 °C		1.3		
Junction & Storage Temperature Range		Tj, Tstg	-55 to 150		°C
Lead Temperature (1/16" from case for 10 sec.)		TL	275		

Note :

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=17.8A

● **Electrical Characteristics** @T_A=25℃ unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	VGS = 0V, ID = 250μA	N-Ch P-Ch	40 -40			V
Gate Threshold Voltage	$V_{GS(th)}$	VDS = VGS, ID = 250μA	N-Ch P-Ch	1.0 -1.0	1.5 -1.6	2.5 -2.5	V
Gate-Body Leakage	I_{GSS}	VDS = 0V, VGS = ±20V	N-Ch P-Ch			±100 ±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V	N-Ch			1	μA
		V_{DS} = -32V, V_{GS} = 0V	P-Ch			-1	
		V_{DS} = 32V, V_{GS} = 0V, T_J = 55 °C	N-Ch			5	
		V_{DS} = -32V, V_{GS} = 0V, T_J = 55 °C	P-Ch			-5	
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 4A	N-Ch		21	30	mΩ
		V_{GS} = -4.5V, I_D = -4A	P-Ch		48	70	
		V_{GS} = 10V, I_D = 6A	N-Ch		16	20	
		V_{GS} = -10V, I_D = -6A	P-Ch		30	45	
Forward Transconductance1	g_{fs}	V_{DS} = 5V, I_D = 12A	N-Ch		14		S
		V_{DS} = -5V, I_D = -6A	P-Ch		12		

DYNAMIC							
Input Capacitance	Ciss	N-Channel VGS = 0V, VDS = 15V, f = 1MHz	N-Ch P-Ch		593 980		pF
Output Capacitance	Coss		N-Ch P-Ch		76 105		
Reverse Transfer Capacitance	Crss	P-Channel VGS = 0V, VDS = -15V, f = 1MHz	N-Ch P-Ch		56 80		
Total Gate Charge2	Qg	N-Channel VDS=20V , VGS=4.5V , ID=6A P-Channel VDS=-20V , VGS=-4.5V , ID=-6A	N-Ch P-Ch		5.5 9		nC
Gate-Source Charge2	Qgs		N-Ch P-Ch		1.25 2.54		
Gate-Drain Charge2	Qgd		N-Ch P-Ch		2.5 3.1		

Turn-On Delay Time2	td(on)	N-Channel VDD = 30V ID ≅ 1A, VGS = 10V, RGEN = 6Ω P-Channel VDD = -30V ID ≅ -1A, VGS = -10V, RGEN = 6Ω	N-Ch P-Ch		11 7	20 14	nS
Rise Time2	tr		N-Ch P-Ch		8 10	18 20	
Turn-Off Delay Time2	td(off)		N-Ch P-Ch		19 19	35 34	
Fall Time2	tf		N-Ch P-Ch		6 12	15 22	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (TC = 25 °C)							
Continuous Current	I_S		N-Ch P-Ch			1.3 -1.3	A
Pulsed Current[3]	I_{SM}		N-Ch P-Ch			2.6 -2.6	
Forward Voltage[1]	V_{SD}	$I_F = I_S$ A, V_{GS} = 0V $I_F = I_S$ A, V_{GS} = 0V	N-Ch P-Ch			1 -1	V

Note :

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=17.8A

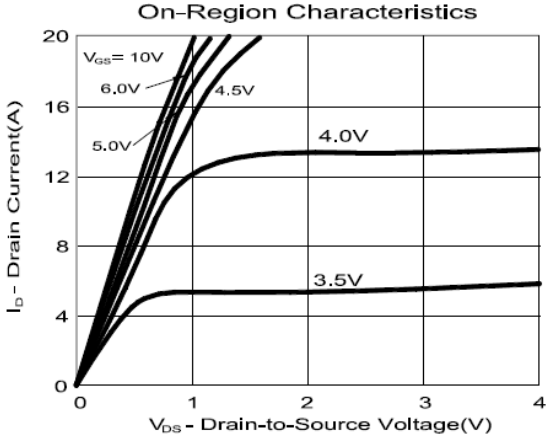
4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

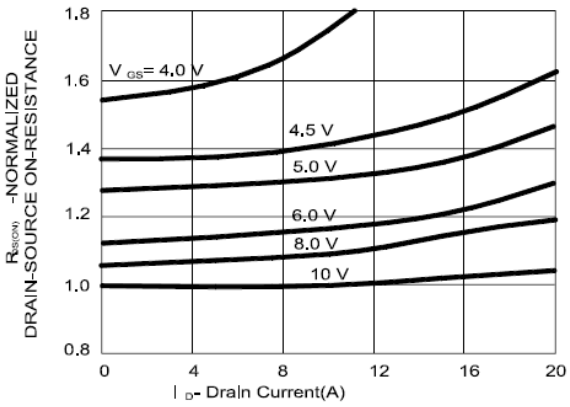
- **Typical Performance Characteristics** (TJ =25 Noted)

N-CHANNEL

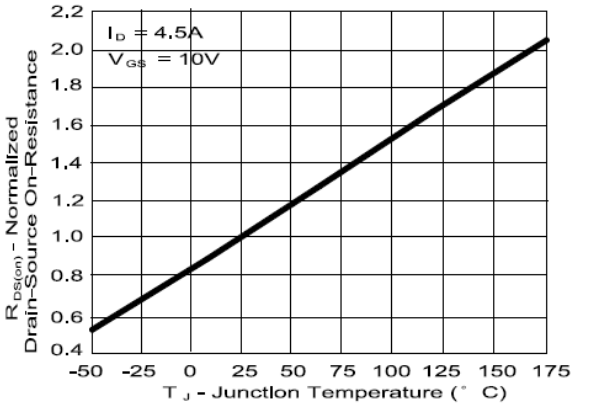
On-Region Characteristics



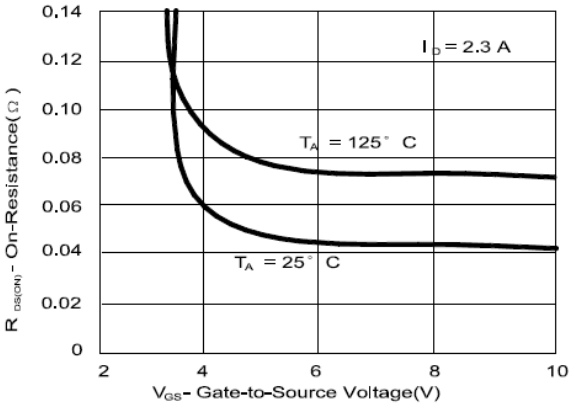
On-Resistance Variation with Drain Current and Gate Voltage



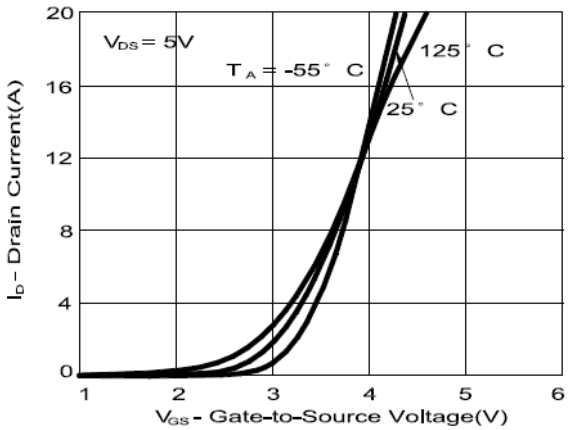
On-Resistance Variation with Temperature



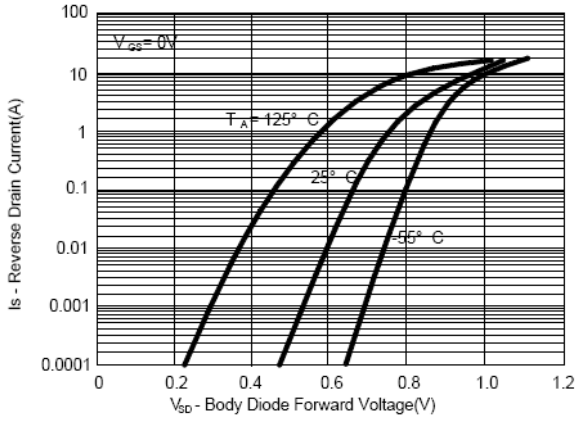
On-Resistance Variation with Gate-to-Source Voltage



Transfer Characteristics

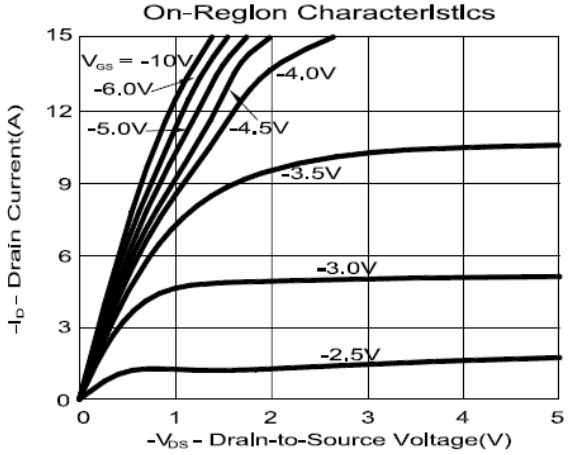


Body Diode Forward Voltage Variation with Source Current and Temp

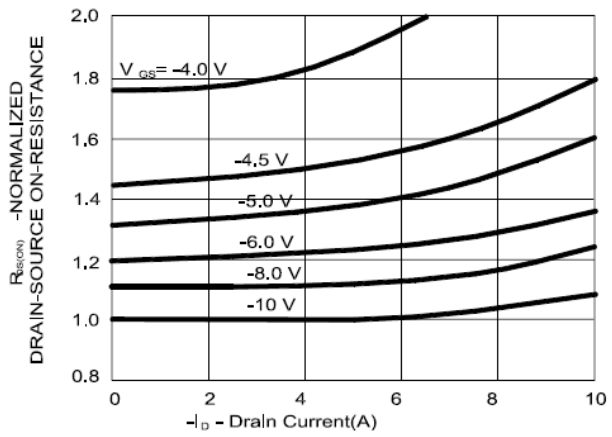


P-CHANNEL

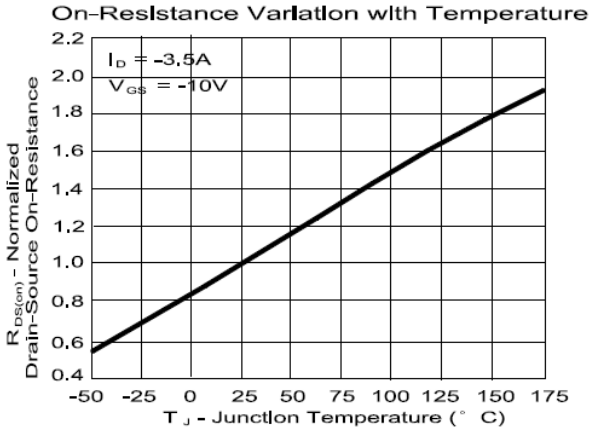
On-Region Characteristics



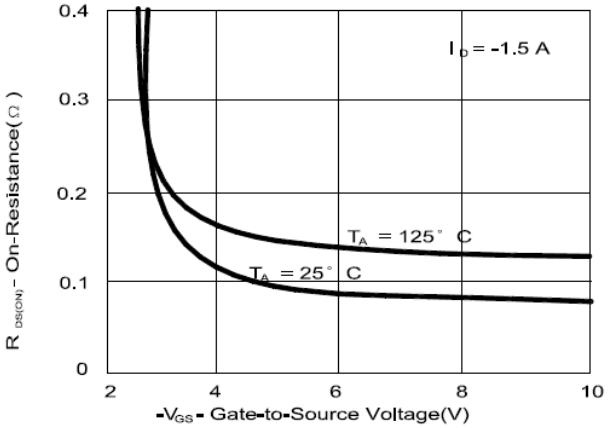
On-Resistance Variation with Drain Current and Gate Volt



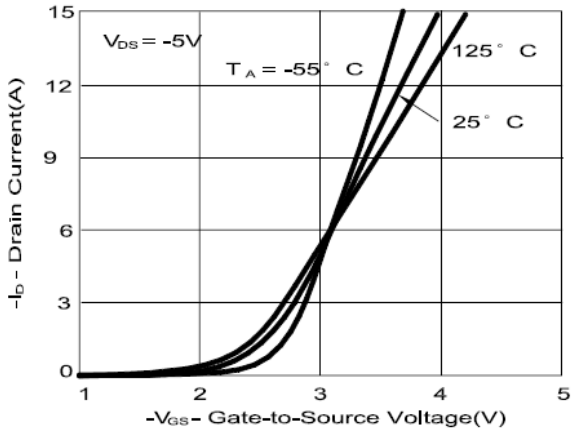
On-Resistance Variation with Temperature



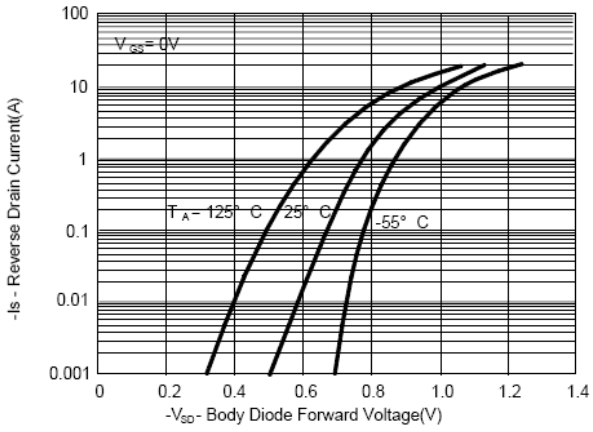
On-Resistance Variation with Gate-to-Source Voltage



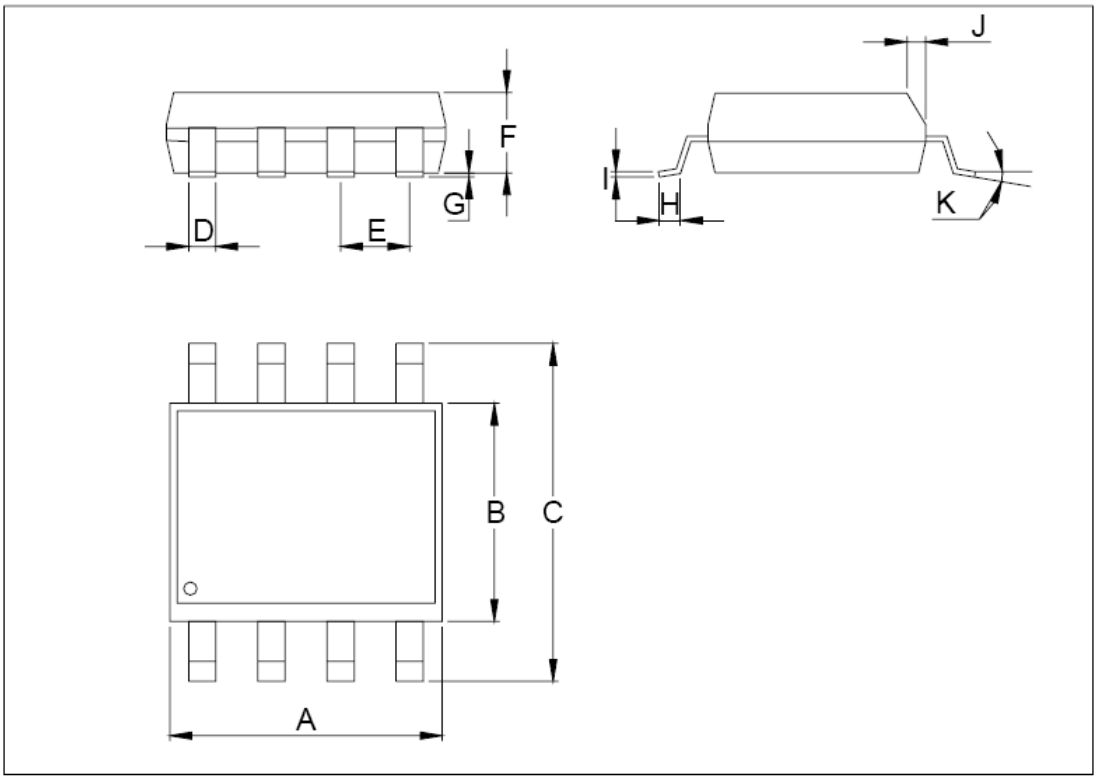
Transfer Characteristics



Body Diode Forward Voltage Variation with Source Current and Temp



SOP8 MECHANICAL DATA



Dimension	mm			Dimension	mm		
	Min	Typ	Max		Min	Typ	Max
A	4.8	4.9	5.0	H	0.5	0.715	0.83
B	3.8	3.9	4.0	I	0.18	0.254	0.25
C	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	K	0°	4°	8°
E		1.27		L			
F	1.35	1.55	1.75	M			
G	0.1	0.175	0.25	N			