100V P-Channel MOSFET

Features

-100V/0.5A ,

$R_{DS(ON)}$ < 2.4Ω @ V_{GS}= - 10V

$R_{DS(ON)}$ < 2.60Ω @ V_{GS}= - 4.5V

Super high density cell design for extremely low $R_{DS(ON)}$

Exceptional on-resistance and maximum DC current capability

Capable doing Cu wire bonding

General Description

The FS2319H is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

APPLICATIONS

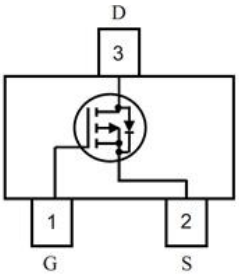
Power Management

Portable Equipment

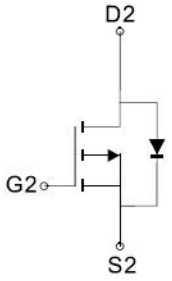
Battery Powered System

Load Switch

Pin Configuration



SOT23-3L



P-Channel MOSFET

Absolute Maximum Ratings (T$_A$=25°C unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(TJ=150_)	Tc=25°C	I_D	-0.5	A
	Tc=70°C		-0.3	
Pulsed Drain Current		I_{DM}	-1.0	A
Continuous Source Current(Diode Conduction)		I_S	-1.0	A
Power Dissipation	TC=25°C	P_D	3.2	W
	TC=70°C		2.1	
Operating Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		$R_{\Theta JA}$	120	°C /W

- **Electrical Characteristics** (TA=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	VGS=0V,ID=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	VDS=VGS,ID=-250uA	-1.0		-2.5	
Gate Leakage Current	I_{GSS}	VDS=0V,VGS=±20V			±10	uA
		VDS=-100V,VGS=0V			-1	
Zero Gate Voltage Drain Current	I_{DSS}	VDS=-100V,VGS=0V TJ=85°C			-30	uA
On-State Drain Current	$I_{D(on)}$	VDS_-10V,VGS=-10V	-0.6			A
Drain-Source On-Resistance	$R_{DS(on)}$	VGS=-10V,ID=-0.5A		2000	2400	mΩ
		VGS=-4.5V,ID=-0.3A		2100	2600	
Forward Transconductance	g_{FS}	VDS=-10V,ID=-0.5A		1.5		S
Diode Forward Voltage	V_{SD}	IS=-0.3A,VGS=0V		-0.75	-1.2	V
Dynamic						
Total Gate Charge	Q_g	VDS=-75V,VGS=-10V ID_-0.5A		4.2	8	nC
Gate-Source Charge	Q_{gs}			0.98		
Gate-Drain Charge	Q_{gd}			1.32		
Input Capacitance	C_{iss}	VDS=-75V,VGS=0V f=1MHz		155		pF
Output Capacitance	C_{oss}			8		
Reverse Transfer Capacitance	C_{rss}			6		
Turn-On Time	$t_{d(on)}$	VDD=-75V,RL=75Ω ID_-1.0A,VGEN=-10V RG=1.0Ω		5	10	ns
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			20	40	
	t_f			10	20	

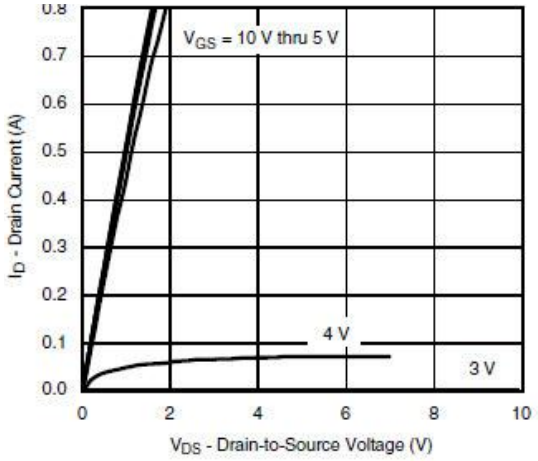
Notes:

a. Based on epoxy or solder paste and bond wire Au or Cu 2mil×2(S), Au or Cu 2mil×1 (G) on each die of SOT-23 (SC-59) package.

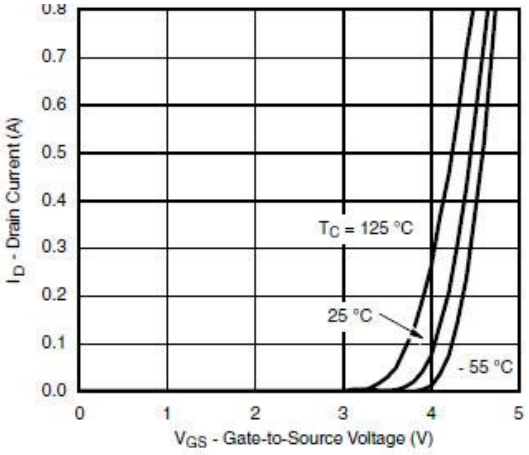
b. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%.

c. Force mos reserves the right to improve product design, functions and reliability without notice.

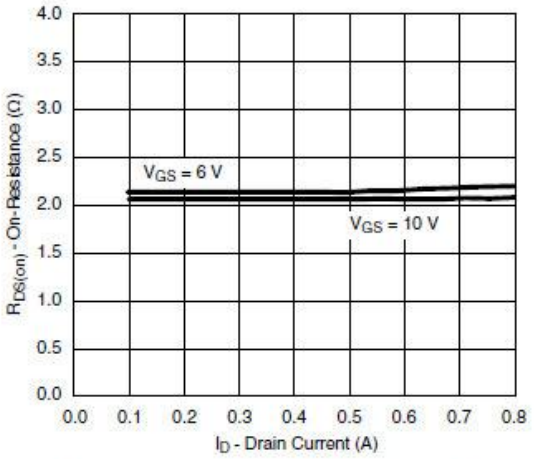
- **TYPICAL CHARACTERISTICS** (25°C UNLESS NOTED)



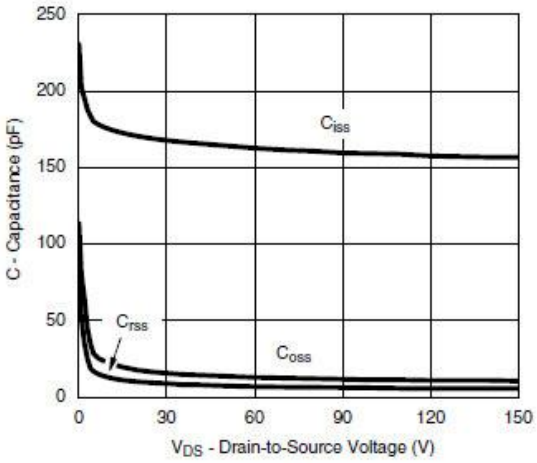
Output Characteristics



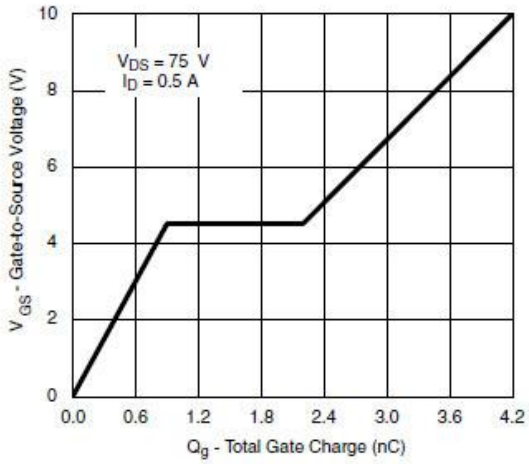
Transfer Characteristics



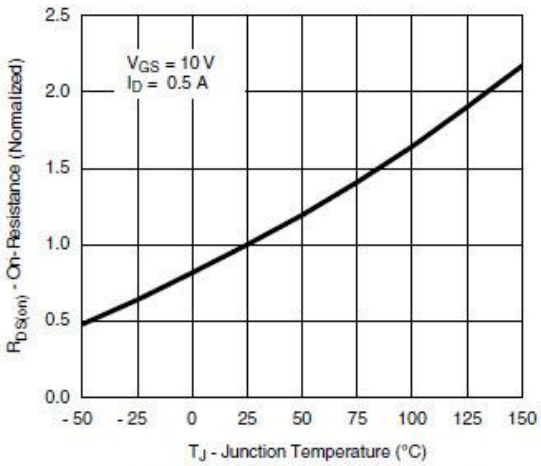
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

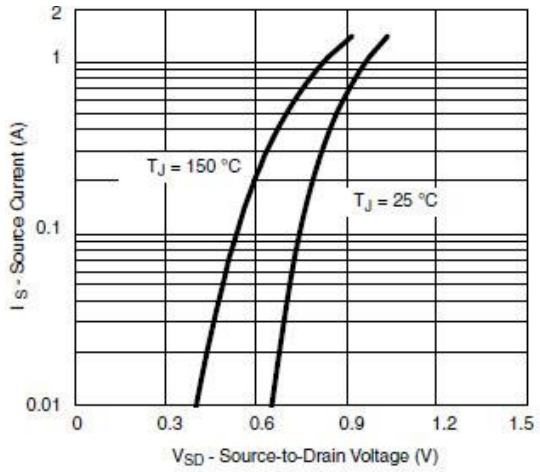


Gate Charge

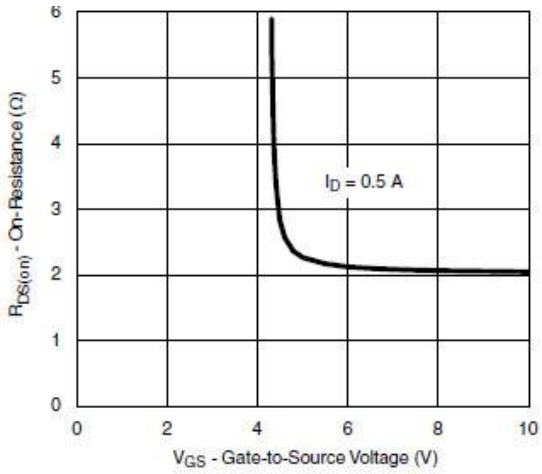


On-Resistance vs. Junction Temperature

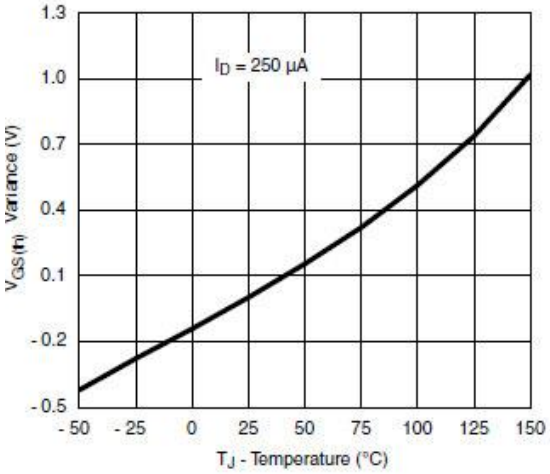
- **Typical Characteristics**



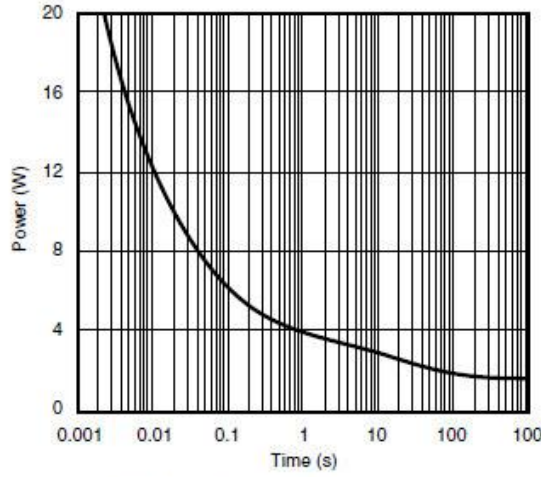
Source-Drain Diode Forward Voltage



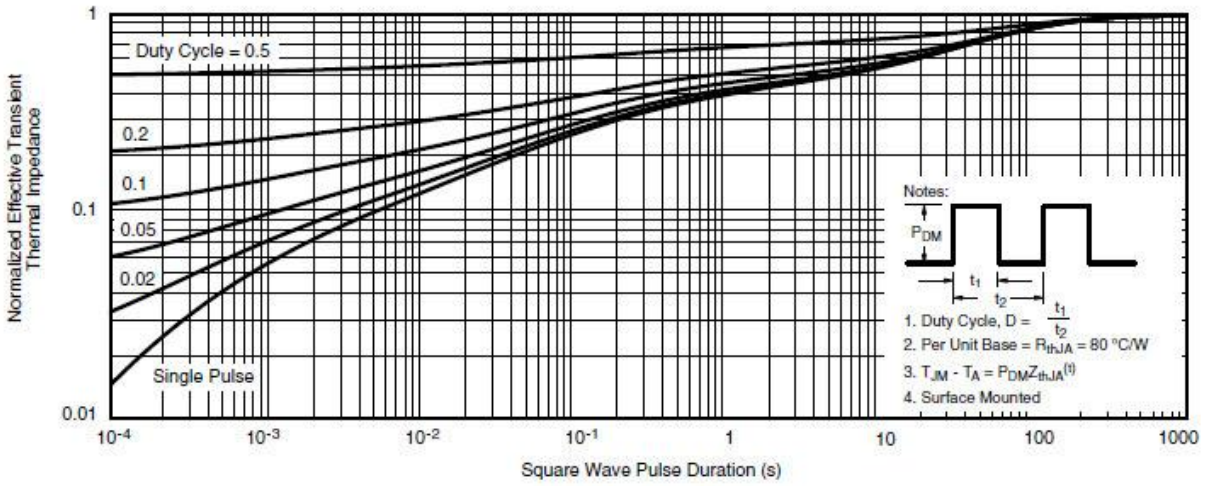
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

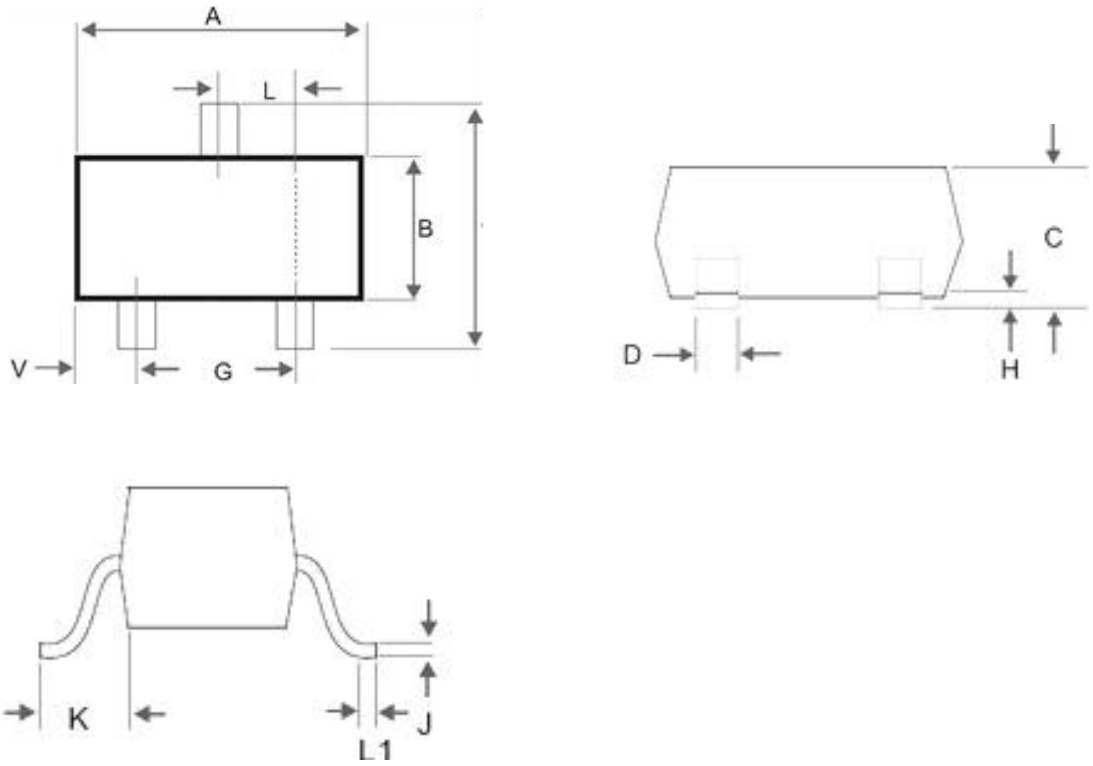


Single Pulse Power, Junction-to-Ambient



- **Package Information**

SOT23-3L



DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.3
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60
L1	0.2	0.6